3030A, 3030C, 3035, 3035C, 3036 (3030 Series) Wideband RF Digitizer PXI Modules

User Manual

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About this manual

This manual explains how to set up and configure an Aeroflex 3030A, 3030C, 3035, 3035C or 3036 wideband RF digitizer PXI module. Where necessary, it refers you to the appropriate installation documents that are supplied with the module.

Please note: this manual applies only when the instrument is used with the supplied software.

This manual provides information about how to configure the module as a stand-alone device. However, one of the advantages of Aeroflex 3000 Series PXI modules is their ability to form versatile test instruments, when used with other such modules and running 3000 Series application software.

Getting Started with afDigitizer (supplied on the CD-ROM that accompanies each module (see Associated documentation)) explains how to set up and configure a 3030 Series RF digitizer with a 3010 Series RF synthesizer module to form a high performance digitizer instrument. Using the digitizer soft front panel and/or dll or COM object supplied, the modules form an instrument that provides the functionality and performance of an integrated, highly-specified RF digitizer, but with the adaptability to satisfy a diverse range of test or measurement requirements.

Intended audience

Users who need to configure and operate wideband RF digitizers to down-convert and digitize RF signals.

This manual is intended for first-time users, to provide familiarity with basic operation. Programming is not covered in this document but is documented fully in the help files that accompany the drivers and associated software on the CD-ROM.

Driver version

To maintain optimum performance, 3000 Series PXI modules should be used either with the software driver version with which they were supplied, or the latest driver, which you can download from the Aeroflex website.

Aeroflex endeavours to ensure modules remain backwards compatible with earlier driver version releases. However, continual improvement means that from software version **6.2.0** onwards there are some exceptions, which are shown in the table below.

Checking the software compatibility of a PXI module

Use this table to check the compatibility of your 3030 Series PXI module with particular versions of software.

- Modules with a serial number label consisting of black lettering on a **white background** (as shown in the 'Serial number' column in the table) are compatible with the minimum driver version shown.

- Modules with a serial number label consisting of black lettering on a **yellow background** (as shown in the 'Serial number' column in the table) are compatible only with software driver version 6.2.0 and higher, as shown in the table.

Please ensure that you install the correct version of software for your module.

Module type	Serial number	Minimum driver version	CD-ROM (46886/028) issue
3030A	Up to 303003/971	5.0.0	9
	From 303003/972	6.2.0	15
3030C	Up to 303006/055	6.1.0	14
	From 303006/056	6.2.0	15
3035	Up to 303004/392	5.0.0	9
	From 303004/393	6.2.0	15
3035C	Up to 303008/473	6.1.0	14
	From 303008/474	6.2.0	15
3036	All modules	6.14.0	26

Option compatibily with release

This table shows which 3030 Series options are compatible with which earliest driver version. Options are then compatible with all driver versions subsequent to that shown.

Option	Description	Compatible with driver version…
100	GSM/EDGE	5.2.0
101	UMTS Uplink	5.2.0
102	CDMA2000 Reverse Link	5.2.0
103	WLAN	5.2.0
104	WIMAX OFDMA	5.4.0
106	Bluetooth	6.3.0
107	LTE (FDD)	6.6.0
108	LTE (TDD)	6.6.0
109	TD-SCDMA	6.6.0
111	Generic Modulation	6.6.0
198	Limit LVDS Data Output Rate	5.4.0

Associated documentation

If you want to…	Refer to…
Find information about soft front panels, drivers, application software, data sheets, getting started and user manuals for this and other modules in the 3000 Series.	**PXI Modules CD-ROM** Part no. 46886/028 Supplied with the module
Install modules into a rack, interconnect them, power up and install drivers.	**3000 Series PXI Modules Common Installation Guide** Part no. 46882/663 On the CD-ROM and at www.aeroflex.com
Set up a populated chassis ready for use.	**3000 Series PXI Modules Installation Guide for Chassis** Part no. 46882/667 On the CD-ROM and at www.aeroflex.com
Set up and use the universal PXI application for system configuration and operation.	**PXI Studio 2 User Guide** Part no: 46892/809 On the CD-ROM and at www.aeroflex.com
Set up and use a digitizer application for 3010 Series and 3030 Series modules *(document currently not maintained — for information only)*.	**Getting Started with afDigitizer** Part no. 46892/676 On the CD-ROM and at www.aeroflex.com
Download example source code	You can download examples of source code (written for different application development environments) from the Aeroflex website.

Preface

The PXI concept

VXI and GPIB systems meet the specific needs of instrumentation users but are often too large and expensive for mainstream applications. PC-based instrumentation may cost less but cannot meet the environmental and operational requirements of many systems.

PXI (PCI Extensions for Instrumentation) is based on CompactPCI, itself based on the PCI standard. PCI was designed for desktop machines but CompactPCI was designed for industrial applications, and features a rugged Eurocard format with easy insertion and removal. PXI adds to the CompactPCI specification by defining system-level specifications for timing, synchronization, cooling, environmental testing, and software. While PXI extends CompactPCI, it also maintains complete interoperability so that you can use any CompactPCI-compliant product in a PXI system and vice versa. PXI also makes use of Windows® software, VXI timing and triggering, and VXIplug&play instrument drivers to provide powerful and affordable systems.

PXI Express now integrates PCI Express into PXI, providing up to 6 Gbyte/s backplane bandwidth and up to 2 Gbyte/s slot bandwidth. PXI Express maintains backwards compatibility with PXI, providing software compatibility and hardware compatibility with hybrid slots and hybrid systems.

Hybrid slot compatibility

PXI chassis that provide hybrid slots can accept both PXI Express modules and hybrid-compatible PXI modules. Hybrid-compatible PXI modules have a ‘missing’ section of connector (see Fig. 1), which allows them to be inserted into both hybrid slots and standard PXI-1 slots.

Because of the reduced connectivity of Aeroflex hybrid-compatible PXI modules, the PXI parallel local bus LBL[0]–[12] disappears, to be replaced by the serial connection LBL[6], which is typically used to provide list addresses to a 3010 Series RF Synthesizer.

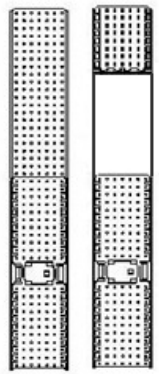


Fig. 1 Standard PXI-1 connector (L) and hybrid-compatible PXI connector (R)

This table shows which Aeroflex wideband RF digitizer PXI modules fit only in a standard slot, and which fit in both hybrid-compatible and standard slots:

3030A	Standard
3030C	Hybrid-compatible and standard
3035	Standard
3035C	Hybrid-compatible and standard
3036	Hybrid-compatible and standard

GENERAL INFORMATION

Introduction

This is the user manual for the 3030A, 3030C, 3035, 3035C and 3036 Wideband RF Digitizers, which are referred to generically in this document as '3030 Series'.

These digitizers operate over the following frequency ranges:

3030A	330 MHz to 3.0 GHz
3030C	250 kHz to 3.0 GHz
3035	330 MHz to 6.0 GHz
3035C	250 kHz to 6.0 GHz
3036	250 kHz to 13.0 GHz

Applications

3030 Series RF Digitizer modules down-convert and digitize RF signals. They convert an analog RF waveform presented at the RF port into a series of amplitude- and phase-corrected digital IF or IQ data pairs at the rear-panel PCI and front-panel data interfaces. Software supplied with the module allows for spectrum analysis of the digitized signals.

3030 Series RF Digitizer modules can be used in RF test and measurement systems used in development or manufacturing. Applications span all areas of radio communications.

Input range and accuracy

Input level control is provided by electronic switched attenuation, which helps to maximize the usable dynamic range. Good level accuracy and repeatability make the module ideal for high-volume manufacturing.

Data capture and processing

Sample data can be output via LVDS in real time, useful for streaming applications. Data can also be captured to internal memory and read out over the PCI bus.

For narrowband signal analysis, the module provides internal digital down-conversion and decimation. Lowering the sample rate allows longer events to be captured. The module contains digital resampling filters that allow you to set the sample rate, as well as numerous preset values associated with common digital communications standards.

Signal routing

A configurable routing matrix provides flexibility in how you interconnect signals on the PXI backplane, the LVDS and TTL front-panel inputs, and the module's internal functions. Predefined routing scenarios can be loaded, or new scenarios created to meet particular requirements.

Triggering and synchronization

The module synchronizes to an external 10 MHz signal (generally supplied by a 3010 Series RF synthesizer). Triggering is external, from the PXI backplane or directly from the front-panel LVDS connector or SMB TTL input, or internal, from the internal timer or level trigger.

List mode

List mode enables very fast settling times for new instrument configurations. In list mode, up to 128 internal hardware settings are pre-calculated and stored, providing fast switching of frequency and level whilst maintaining RF output accuracy. List addresses are sourced externally or from an internal counter driven by the test application controlling the 3030 Series module.

Software

A 3030 Series module is supplied with a VXI PNP driver and soft front panel for use as a standalone module. It is also supplied with an instrument-level signal generator soft front panel, a dll, a COM object, and a .net assembly for use with a 3010 Series RF synthesizer.

PXI Studio 2, supplied with the module, configures your PXI modules as logical instruments using an intuitive and powerful graphical interface. PXI Studio 2 provides comprehensive signal generator, digitizer and spectrum analyzer applications and optional analysis plugins to suit specific communications systems.

Deliverable items

- 3030 Series Wideband RF Digitizer PXI module
- PXI Modules CD-ROM (part no. 46886/028), containing soft front panels, drivers, application software, data sheets, installation guides, safety instructions, getting started and user manuals for this and other modules in the 3000 Series
- Test results and calibration certificate CD-ROM part no. 46886/054
- *3000 Series PXI Modules Safety Instructions*: printed item, part no. 46882/882
- SMA connector cable: part no. 43139/738; 2 off for 3030A/3035 and 1 off for 3030C
- SMA connector cable: part no. 43139/739; 1 off for 3035C/3036

Cleaning

Before commencing any cleaning, switch off the chassis and disconnect it from the supply. You can wipe the front panel of the module using a soft cloth moistened in water, taking care not to wet the connectors. Do not use aerosol or liquid solvent cleaners.

Putting into storage

If you put the module into storage, ensure that the following conditions are not exceeded:

Temperature range:	–20 to +70°C (–4 to +158°F)
Humidity:	5 to 93%, non-condensing

Specifications

For the latest specifications, see the data sheet included on the CD-ROM (part no. 46886/028) or go to the Aeroflex website.

All 3030 Series specifications are defined when used in conjunction with the 3010/11 RF Synthesizer PXI module and driver software supplied with the module.

Warm-up time

Allow at least twenty minutes for a module to warm up and meet its specifications fully after booting.

Calibration and servicing

The recommended calibration interval is 24 months.

There are no user-serviceable parts in these modules; if any attention is needed, return the module to your Aeroflex agent.

INSTALLATION

WARNING

Initial visual inspection

Refer to the *3000 Series Common Installation Guide* part no. 46892/663 on the PXI Modules CD-ROM, part no. 46886/028.

Hardware installation

WARNING

Before installing the module into the chassis, check that:

(a) no foreign conductive bodies are present between pins on the backplane or module connectors

(b) no pins on the backplane or module connectors are bent or damaged.

(c) the PXI backplane slot arrangement is compatible with the module.

WARNING

Take care when touching a module which has run for a prolonged period; the surface temperature can become high.

CAUTION

Airflow

Fit slot blockers to all unused slots. Modules can overheat if the correct airflow is not maintained.

CAUTION

Handling precautions

Refer to the *3000 Series Common Installation Guide* part no. 46892/663 on the PXI Modules CD-ROM, part no. 46886/028.

Installing the module into the PXI chassis

Refer to the *3000 Series Common Installation Guide* part no. 46892/663 and *Installation Guide for Chassis* part no. 46882/697 on the PXI Modules CD-ROM, part no. 46886/028.

These guides provide information such as specific precautions to take, positioning and fitting the modules, making connections for the LO and the 10 MHz reference signal, installing hardware drivers, and so on.

Connector care and maintenance

How to connect and torque an SMA connector

1 First, ensure that the mating halves of the connector are correctly aligned.

2 Next, engage the threads of the nut and tighten it by hand, ensuring that the mating halves do not move relative to each other.

3 Then use a torque wrench to tighten the connector, in order to ensure consistent matching and to avoid mechanical stress.

Torque settings for connectors are:

0.56 Nm test torque (development use, semi-permanent installations)

1 Nm final torque (permanent installations)

Never use pliers to tighten connectors.

CAUTION

Overtightening will cause damage!

Do not allow center pins to rotate!

Do not allow the center pins of connectors to rotate when you connect and remove cables.

Use a connector saver!

Use a connector saver (part no. 46885/224):

(a) on any SMA connector where the cable is routinely connected and disconnected

(b) when the connector on the cable, or the cable end of the connector saver, has not been gauged.

Torque to 1 Nm the end of the connector saver that connects to the module, and torque to 0.56 Nm the end that connects to the cable.

Maintenance

SMA

Clean connectors regularly, using a cotton bud dipped in isopropyl alcohol. Wipe within the connector cavity, then use a dry cotton bud to finish off. Check for any deposits.

Do not use other cleaners, as they can cause damage to the plastic insulators within the connectors.

Cap unused connectors.

PCI

Protect PCI connector pins by keeping modules in their original packing when not fitted in the rack.

OPERATION

Front-panel connectors

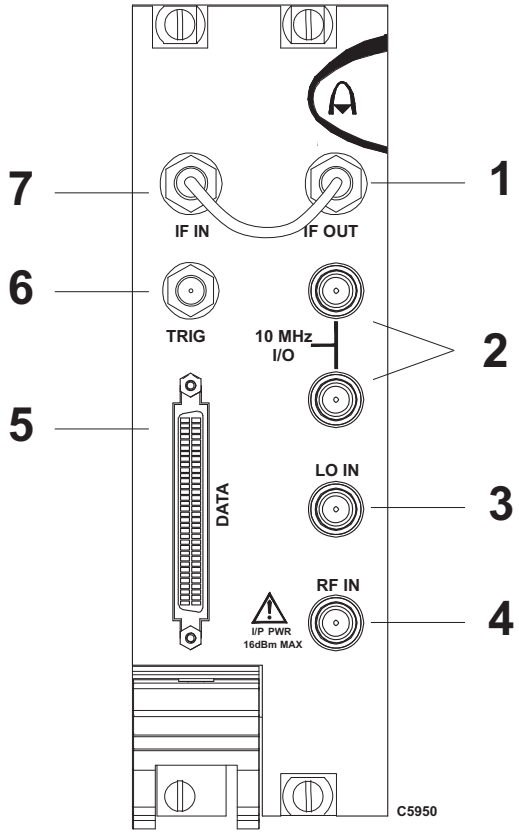


Fig. 2 ***3030A, 3035*** *front panel*

1	IF OUT	77.76 MHz. SMA socket, 50 Ω.
2	10 MHz I/O	Two SMA I/O sockets in parallel. **Input** Ext frequency standard input for sampling clock. 1.0 to 4 V pk-pk into 50 Ω. **Output** Link-through from input.
3	LO IN	1.5 to 3 GHz, nominally 0 dBm. SMA socket, 50 Ω.
4	RF IN	SMA socket, 50 Ω.
5	DATA	68-way VHDCI connector for LVDS data I/O, 14-bit IQ digital data output. See Data connector for details.
6	TRIG	TTL +ve or -ve edge. SMB socket, 50 Ω.
7	IF IN	77.76 MHz input. SMA socket, 50 Ω.

CAUTION

Maximum safe power at RF input

3030A: **+22 dBm** (8 dB minimum input attenuation)

3035: **+30 dBm** (10 dB minimum input attenuation, 10 dB IF attenuation)

Maximum safe power at IF input

3030A, 3035: **+10 dBm** (0 dB IF attenuation)

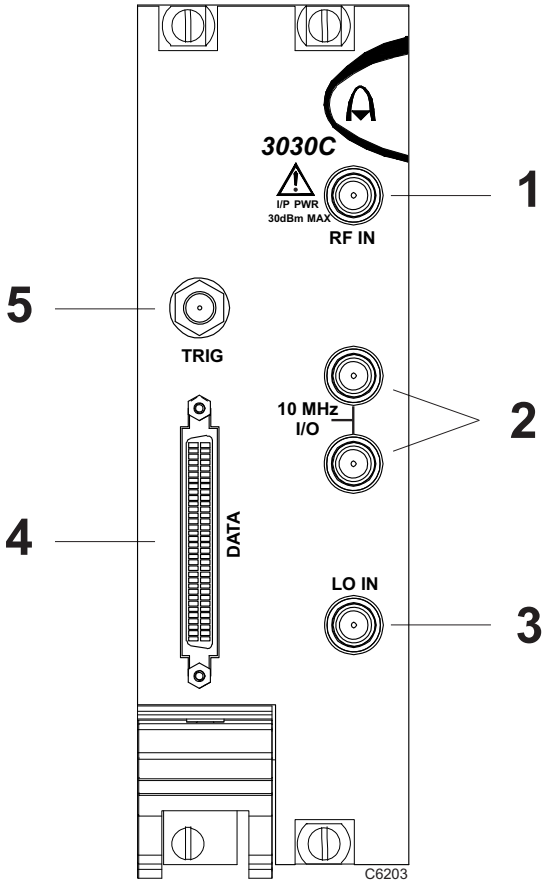


*Fig. 3 **3030C** front panel*

1	RF IN	SMA socket, 50 Ω.
2	10 MHz I/O	Two SMA I/O sockets in parallel. **Input** Ext frequency standard input for sampling clock. 1.0 to 4 V pk-pk into 50 Ω. **Output** Link-through from input.
3	LO IN	1.5 to 3 GHz, nominally 0 dBm. SMA socket, 50 Ω.
4	DATA	68-way VHDCI connector for LVDS data I/O, 14-bit IQ digital data output. See Data connector for details.
5	TRIG	TTL +ve or –ve edge. SMB socket, 50 Ω.

CAUTION **Maximum safe power at RF input +30 dBm** (10 dB minimum input attenuation)

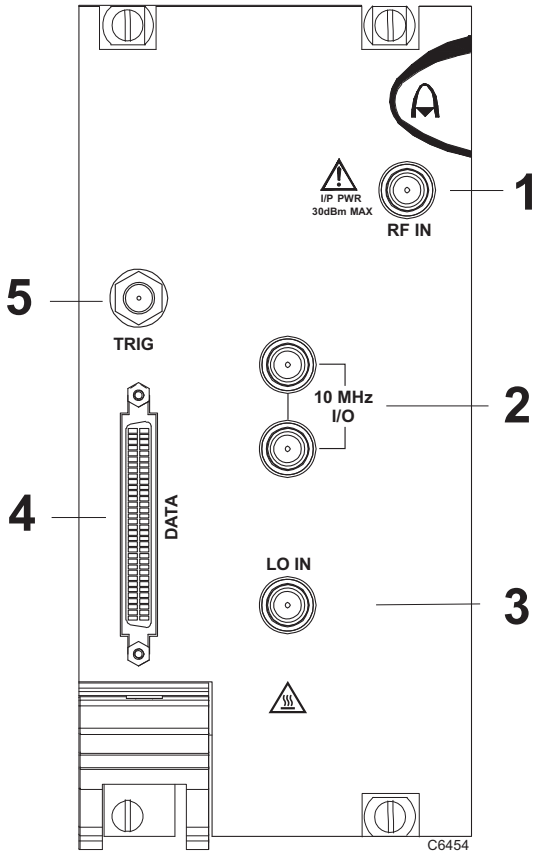


Fig. 4 ***3035C, 3036*** *front panel*

1	RF IN	SMA socket, 50 Ω.
2	10 MHz I/O	Two SMA I/O sockets in parallel. **Input** Ext frequency standard input for sampling clock. 1.0 to 4 V pk-pk into 50 Ω. **Output** Link-through from input.
3	LO IN	1.5 to 3 GHz, nominally 0 dBm. SMA socket, 50 Ω.
4	DATA	68-way VHDCI connector for LVDS data I/O, 14-bit IQ digital data output. See Data connector for details.
5	TRIG	TTL +ve or –ve edge. SMB socket, 50 Ω.

CAUTION **Maximum safe power at RF input** **+30 dBm** (10 dB minimum input attenuation)

Soft front panel (af3030_sfp)

The soft front panel provides a graphical interface for operating the module. It is intended for testing and diagnosing, for demonstration and training, and for basic operation of the module. It represents most of the functions available in the instrument driver. It is not, however, a comprehensive application suitable for measurements; for this, use the afDigitizer dll, the afcomDigitizer COM object, the .net assembly (afDigitizerDotNet.dll) or PXI Studio 2.

Installation

The soft front panel is installed during the driver installation process (refer to the *3000 Series PXI Modules Common Installation Guide*, part no. 46882/663, on the PXI Modules CD-ROM).

Access the soft front panel from the Windows Start menu under *Programs\Aeroflex\PXI Module Front Panels\AF3030 Soft Front Panel*. Or open the *af3030_sfp.exe* file, which if you did not change the default location, is located with the VISA software. The soft front panel, similar to that in Fig. 5, is displayed.

Detailed help information

Soft front panel controls are all available as driver export functions unless noted otherwise, and are documented in the help files. This user manual provides an overview of the facilities that the module provides and summarizes its operation; however, refer to the help files for detailed descriptions of functions, together with their parameter lists and return values.

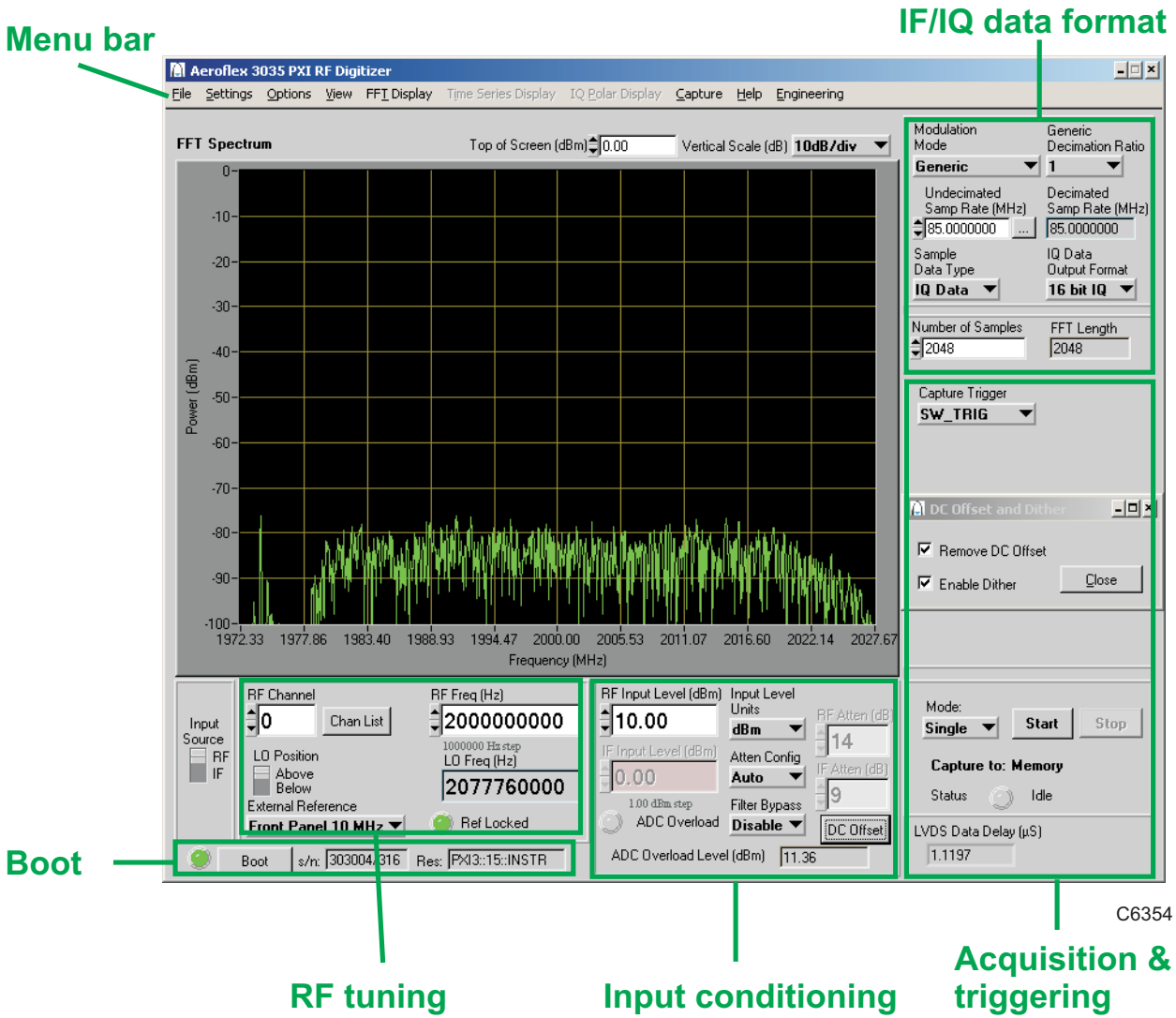


Fig. 5 3035 soft front panel (other 3030 Series are similar)

Menu bar

File

Save Captured Data (as ASCII file)… captures the 16-bit sample data into the specified ASCII file.

Save Captured Data (as Binary file)… captures the 16-bit sample data into the specified binary file.

Click **File\Exit** on the menu bar to close the application.

Settings

Settings\Load and **Settings\Save** on the menu bar allow you to load and save soft front panel configurations from and to your preferred locations. If you did not change the default location when installing the software, it is the same as for the VISA software (refer to the *3000 Series PXI Modules Common Installation Guide* for details), and configurations are saved as *.ini* files.

> You can edit, copy and paste settings files as required; for example, you may want to save only a new routing setup without changing other parameters. Edit the saved *.ini* file using a text editor (for example, Notepad) to remove unwanted parameters. Ensure only that you do not delete the General (VendorID, DeviceID) and Version (Major/Minor) parameters. Save the changed file. When the settings file is next loaded, the configuration of the soft front panel changes to match the parameters remaining in the settings file, leaving all other settings unchanged.

Settings\Directories on the menu bar lets you choose the default directory for your front-panel configuration settings.

Settings\LVDS on the menu bar allows you to set:

- **Clock Rate**: the LVDS clock rate, choice of 180 MHz, 125 MHz (default), 62.5 MHz.
- Each LVDS **Data**, **Auxiliary** and **Marker** mode for input, output or tri-state (default) operation.

  Spare 0 is controlled by LVDS Data Mode. To use Spare 0 as a trigger input, set LVDS Data to Input. To use Spare 0 as a trigger output, set LVDS Data to Output.

  To use an auxiliary bit as a trigger input, set LVDS Auxiliary to Input. To use an auxiliary bit as a trigger output, set LVDS Auxiliary to Output.

  To use a marker bit as a trigger input, set LVDS Marker to Input. To use a marker bit as a trigger output, set LVDS Marker to Output.
- **IF Data Position**: places 14-bit IF data in either the upper 14 bits of a 16-bit word (the lower two bits are padded with 0s) or lower 14 bits of a 16-bit word (upper two bits are sign extended), as required by the processing software.

Settings\Timer… on the menu bar allows you to configure the internal timer.

Settings\List Mode… on the menu bar allows you to configure list mode settings.

Settings\Routing Scenarios on the menu bar allows you to select a predefined routing matrix connection. A tick against the scenario's title shows that it is selected.

Selecting or removing a routing scenario affects only the connections specific to that scenario, and does not change any other routing connections. However, changing the routing matrix connections of any scenario invalidates that scenario.

Settings\Routing Matrix on the menu bar displays a matrix that provides interconnection between input and output signals on the PXI backplane bus, the DATA connector, the TRIG connector and the module's internal circuitry, as shown diagrammatically in Fig. 6. This provides great flexibility in how you can route signals between modules.

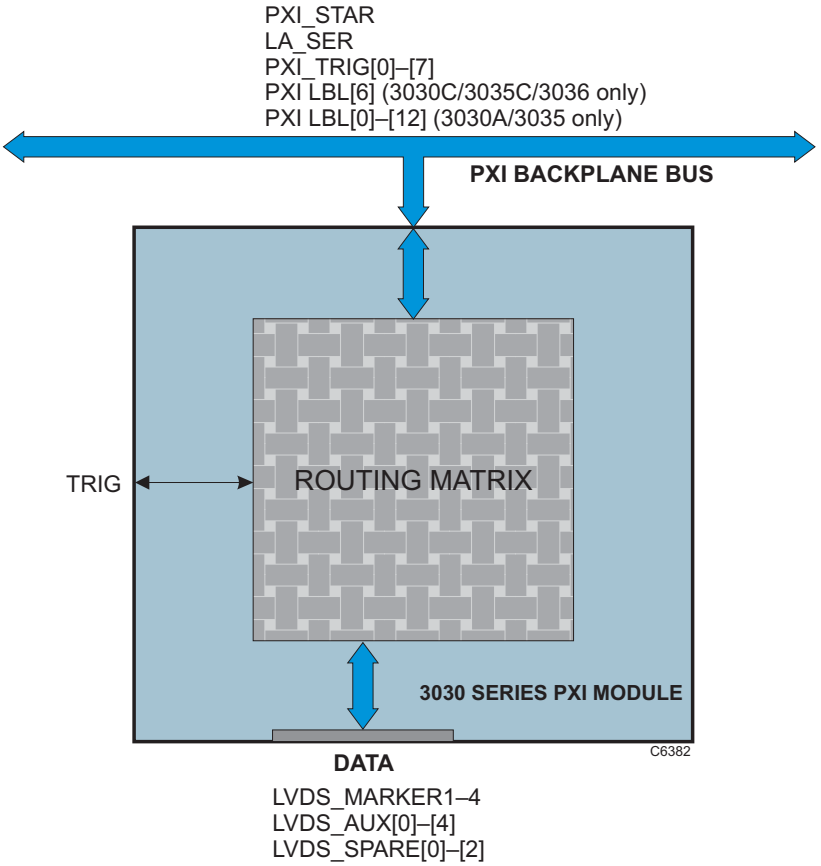


Fig. 6 Routing matrix in 3030 Series

Routing matrix

Use the routing matrix (Fig. 7) to interconnect signals. Output signals form the body of the matrix. Select appropriate input signals from the drop-down menus under each down-arrow to create the interconnections.

Check the boxes to enable the outputs and select the appropriate LVDS mode.

Reset sets all input signals to GND and disables the outputs (LVDS outputs go tri-state). This is the default state.

When operating the module in default digitizer mode (routing matrix reset), all necessary input, output and trigger signals are available on front-panel DATA, SMA and SMB connectors and there is no need to configure the matrix. If you need to set up particular signal routings, you can define these using the drop-down menus on the matrix and save them using the **Settings\Load** and **Save** commands in **Settings**, or use **Settings\Routing Scenarios** to access pre-set alternative routings, or contact Aeroflex if you need assistance in defining particular routing requirements.

3030 Series are hybrid slot-compatible PXI-1 peripheral modules, and so all but one of the parallel LBL outputs are grayed out and unavailable. Instead, the drop-down menu associated with LBL[6] provides a serial interface LA_SER.

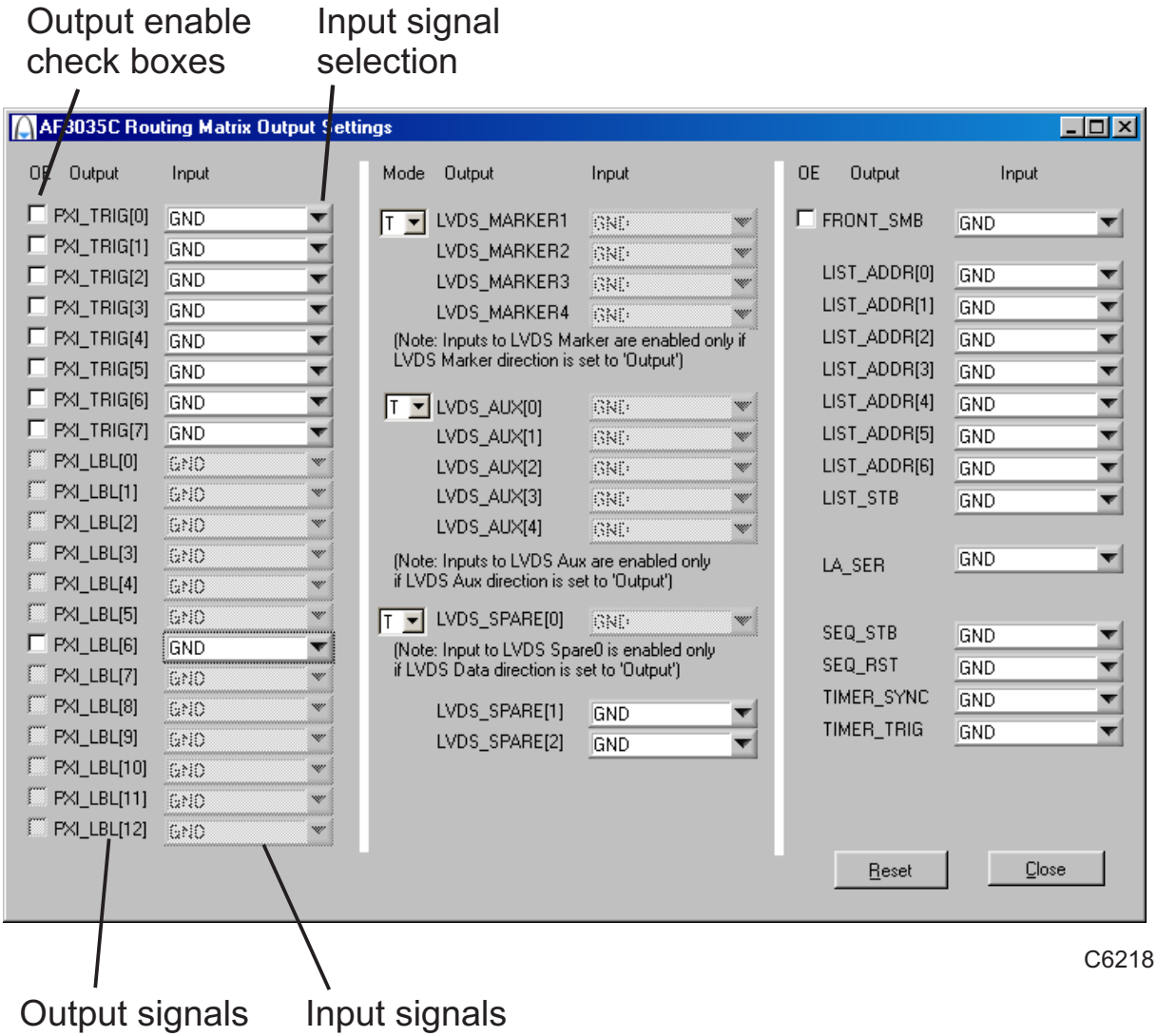


Fig. 7 Routing matrix inputs and outputs (other 3030 Series are similar)

Routing matrix signals are shown in the following tables. All signals are active high. Note that some signals apply to 3030C/3035C/3036 or 3030A/3035 only.

***Note**: the labels shown below are prefixed af3030_ROUTE_ when using af3030_32.dll (see af3030_lib_const.h). If using afdigitizer (preferred), the labels are prefixed afDigitizerDll_rm (see afdigitizer help file).*

Routing matrix data destinations: external signals		
Name in SFP	**Label**	**Description**
PXI_TRIG[0]–[7]	PXI_TRIG_N	Eight PXI bus timing and trigger lines (TTL) shared by all modules, which allow one card to co-ordinate the actions of others. Recommended to keep signals below 20 MHz. Each output can be enabled individually.
PXI_LBL[0]–[12] *3030A/3035 only*	PXI_LBL_N	13 parallel PXI local bus lines to the adjacent slots on the left of the module. LBL[0]-[7] are typically driven from LA_OUT[0]-[7] to route the list address to an associated 301x module.
PXI_LBL[6] *3030C/3035C/3036 only*	PXI_LBL_6	Only LBL[6] is available on PXI hybrid modules. This is typically used to route the list address to an associated 301x by driving it from the serial list address, LA_SER.
LVDS_MARKER[1]–[4]	LVDS_MARKER_N	Four LVDS marker bus lines on the front panel LVDS connector. When enabled, all four bits are outputs.
LVDS_AUX[0]–[4]	LVDS_AUX_N	Five LVDS auxiliary bus lines. When enabled, all five bits are outputs.
LVDS_SPARE[0]	LVDS_SPARE_0	Spare LVDS line 0. Setting all the LVDS data lines to outputs enables SPARE_0. LVDS lines are tristate.
LVDS_SPARE[1], LVDS_SPARE[2]	LVDS_SPARE_N	Spare LVDS outputs. LVDS_SPARE_1 and LVDS_SPARE_2 are output only.
Front SMB	FRONT_SMB	Front panel trigger. Acts as output when enabled.

Routing matrix data destinations: internal signals		
Name in SFP	**Label**	**Description**
LIST_ADDR[0]–[7]	LA_IN_N	Selects the list address (parallel mode – also requires LIST STB to be assigned).
LIST_STB	LSTB_IN	List address strobe input (used for parallel mode only)
LA_SER	LA_SER	Selects the list address (serial mode — requires only one control line).
SEQ_STB	SEQ_STB	Strobe signal to internal list counter.
SEQ_RST	SEQ_RST	Resets the internal list counter.
TIMER_SYNC	TIMER_SYNC	Restarts the internal timer.
TIMER_TRIG	TIMER_TRIG	External trigger for the internal timer.

Routing matrix data sources: external signals

Note that, in general, bidirectional external signals that have been enabled as outputs can still be used as a data source.

Name	Label	Description
PXI Trigger[0]–[7]	PXI_TRIG_N	Signals from the PXI Trigger bus.
PXI Star Trigger	PXI_STAR	Dedicated trigger line from the module in slot 2. Input only. Can be used to trigger multiple modules independently with low timing skew.
PXI Local Bus Left *3030A/3035 only*	PXI_LBL[0:12]	13 parallel PXI local bus lines from the adjacent slot on the left of the module. Generally used to drive the list address *to* 301x and not commonly used as a data source.
PXI Local Busy Left bit 6 *3030C/3035C/3036 only*	PXI_LBL–[6]	Only LBL[6] is available on PXI hybrid modules.
LVDS Markers	LVDS_MARKER[1:4]	Four marker bits from the front panel LVDS connector.
LVDS Auxiliaries	LVDS_AUX[0:4]	Five aux bits from the front panel LVDS connector.
LVDS Spare 0	LVDS_SPARE_0	Single spare bit from the front panel LVDS connector.
Front Panel SMB	FRONT_SMB	Data from front panel trigger connector.

Routing matrix data sources: internal signals		
Name	**Label**	**Description**
Internal Trigger	INT_TRIG	Internal level trigger selected by internal trigger mode (absolute or relative). See INT_TRIG.
Internal Timer	TIMER	Internal timer output. See INT_TIMER.
Capture Busy	CAPT_BUSY	Data capture active.
Sequencer	SEQ_OUT_[0:7]	Internal counter output. The counter resets with SEQ_RST and increments on the rising edge of SEQ_STB.
Sequencer Strobe	SEQ_STB_OUT	Internal counter strobe output.
List Address Output	LA_OUT_[0:6]	The currently selected list address in parallel form. These signals are typically routed via PXI_LBL_N to an associated 301x to command it to the same list address.
Sequencer Start	SEQ_START	Indicates start of counter sequence
Software Trigger	SW_TRIG	Software trigger signal.
Serial List Address	LA_SERIAL_OUT	Serial form of LA_OUT list address. This can be used to reduce the number of pins required to communicate the list address. It is generally used on hybrid modules to send the list address to the associated 301x via PXI_LBL_6.
Ground	GND	Logic zero.

Settings\Optimization on the menu bar allows you to choose how the module compensates for the effect of temperature changes and RF frequency response.

Auto Temperature Optimization (default) monitors the temperature of the module at regular intervals and adjusts the correction figure for the current temperature. You can turn this off if it might interfere with a time-critical measurement. It is also turned off automatically when List Mode is enabled.

Optimize Temperature Correction forces an immediate update, after which the timer starts a new interval.

Auto Flatness Mode compensates for the slope of the RF response, and may be needed for measurements taken over a wide bandwidth. It applies compensation to 'flatten' the response over the chosen bandwidth. Default is 'off'.

Enable Pre-Amp Control, when selected, allows you to switch in the preamp at low signal levels.

Options

Allows you to enable or disable additional instrument options if you have the appropriate password (available from the Aeroflex sales desk). Click **Options\Edit…** on the menu bar to display the options screen (Fig. 8).

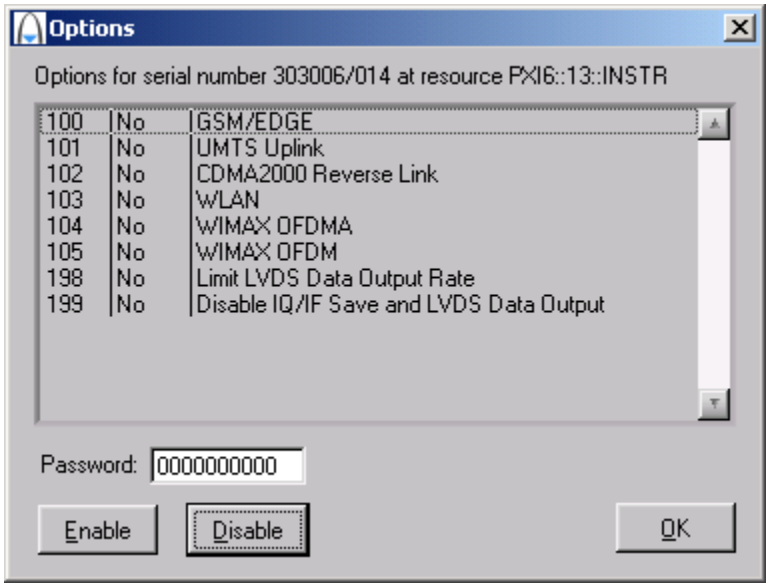


Fig. 8 Options screen

Disabled options are shown grayed out. To enable an option, enter the appropriate password. Click **Enable**. The enabled option is shown highlighted in green. Click **OK**.

View

Allows you to view results in different formats.

View FFT (default) displays a single graph showing logarithmic power versus frequency. The default span is 66% of full span. You can modify the top of screen reference power (dBm) and the vertical scaling (dB/div). Select other display settings from FFT Display.

View Time Series displays two graphs showing I and Q magnitude (in IQ mode) or IF magnitude (in IF mode) versus sample number. Sample Start and Sample End let you change the start and stop time of samples, allowing you to 'zoom in' on data. Select other display settings from Time Series Display.

View IQ Polar presents I and Q data as a polar response. Select other display settings from IQ Polar Display.

View Numeric Data displays IQ or IF data that can be placed alongside either the FFT or Time Series views. Numeric data representing the values of I and Q capture data is displayed as I first, followed by Q. Use the scroll bar to inspect long sample records.

FFT Display

This menu is enabled only when View\View FFT is selected. It allows you to hide/display the graticule and save the dB levels of the trace as a *.txt* or other file.

Graticule Visible hides or displays the graticule.

The **Span** menu selects either Full or Truncated (approx. 66%) span. For example, with Modulation Mode set to UMTS and with a Decimation Ratio of 2, Full span is the full decimated bandwidth of the module (30.72 MHz) and Truncated limits this to 20 MHz, placing graticule lines at integer frequencies for easier reading.

For Generic Modulation Mode, the Full and Truncated limits are 51.84 MHz and 33 MHz respectively (3030A/3035) or 125 MHz and 81.38 MHz respectively (3030C/3035C/3036), reflecting the maximum available span of the module with a Decimation Ratio of 2.

Save FFT Trace saves the current FFT trace as a text file. The FFT trace is recorded as an array of dB values. The length of the array is displayed in the FFT Length field. The text file's location is defined in File Setup...

File Setup… allows you to select the filename and location for the FFT trace.

Time Series Display

When **View Time Series** is selected, the Time Series Display menu is enabled, allowing you view I and Q traces on two separate graphs or overlaid in different colors.

Graticule Visible hides or displays the graticule.

IQ Separate Graphs displays separate graphs of Time Series (I) and Time Series (Q). Both graphs are displayed with a common horizontal axis scaling (as set by Sample Start and Sample End).

IQ Overlaid Graph displays colored I and Q traces on a single graph; I is yellow and Q is green.

IQ Power Graph displays the instantaneous magnitude of $\sqrt{I^2+Q^2}$.

Full Width Sample View adjusts the number of samples displayed in the graph to the number of samples captured.

Y-axis Autoscale: when selected, automatically sets the scaling of signal magnitude to the peak value. When it is deselected, you can set the values manually using the Magnitude Min and Magnitude Max controls above the display. The values of Magnitude Min and Magnitude Max apply to both I and Q when IQ Separate Graphs is selected.

IQ Polar Display

When **View IQ Polar** is selected, the IQ Polar Display menu is enabled, allowing you view I and Q traces on a polar plot.

Graticule Visible hides or displays the graticule.

Autoscale, when selected, scales the I and Q signal magnitudes to the peak value. When it is deselected, you can set the values manually using the IAxis Range (±) and QAxis Range (±) controls above the display.

Capture

By default, the module captures data to the screen (**To Screen Only**), but you can also capture results to ASCII or binary files whilst continuing to display on screen (**To ASCII File and Screen**; **To Binary File and Screen**).

File Setup… opens a browser to define a file extension (default is *.txt*) and location for storing data. Files are saved as interleaved I/Q pairs (I followed by Q) or single IF data, depending on the setting of the Sample Data Type field.

- ASCII IQ file: I and Q values are on new lines, I value followed by Q value.
- Binary IQ file (16-bit mode): I and Q values are stored as 16-bit integers, I value followed by Q value.
  Binary IQ file (32-bit mode): I and Q values are stored as 32-bit integers, I value followed by Q value.

Help

Instrument Information provides the module's PXI resource code and serial number, revision numbers for driver, FPGA and PCI, and its last calibration dates.

About provides the version and date of the soft front panel.

Boot

Click **Boot** (here) to initialize the module and view the Boot Resource window. Resources available for initializing are shown in blue.

Select the 3030 Series module you want to boot.

Boot default FPGA configuration box.
Check this. Do not change the configuration unless you are advised otherwise.

EEPROM caching box.
Ignore for 3030C/3035C/3036 (has no effect).

3030A/3035: check this, so that when you boot a particular module for the first time, calibration data is read from the module and placed in the local cache that you define in the EEPROM Cache Path. This initial boot time is of the order of 45 seconds. Then check the EEPROM caching box at subsequent power-ups of this module to provide considerably faster boot times. The EEPROM caching box is cleared at each power-down.

Click **OK**. While you select the boot resource, the indicator is amber. Once the module has initialized, the indicator changes to green in a few seconds.

If no calibration data is available, the driver returns a caution. If this happens, return the module for calibration.

Note: *in earlier versions of software (up to and including v6.12.0), if you boot the module with EEPROM caching disabled and then enable a new option, the option is not recognized after a subsequent reboot with caching enabled. The solution is to ensure that EEPROM caching is enabled before enabling a new option. Subsequent versions of software ensure that the ability to enable options is independent of the EEPROM caching setting.*

s/n:

After the module initializes, this field displays its serial number.

Res:

After the module initializes, this field displays its VISA resource string.

RF tuning

RF Channel

Sets the currently active channel in a range of 0 to 127.

Chan List

Click this to set up the channels for list mode operation. You can Load and Save the settings file to make setup easier.

RF Freq (Hz)

This is the RF input frequency. This defines the center frequency of the FFT trace and selects appropriate correction values.

The module is tuned by setting the RF frequency and the LO offset direction (above or below). From these two values, the module calculates the LO frequency that must be applied to the LO input.

Set the input frequency using the up/down arrows or by entering the frequency in Hz or scientific (e) notation.

LO Position

Displays the local oscillator position relative to the RF frequency.

Set to Above to make the LO higher than the RF, and to Below to make the LO lower than the RF. For some frequencies, LO Position is fixed and cannot be changed.

LO Freq

Shows the frequency to which a 3010 Series RF synthesizer module or other source should be set in order to provide the correct LO frequency for the 3030 Series module. If you are using a 3010 Series module, simply double-click on the field, copy the value, and paste it into the RF Frequency (Hz) field on the 3010 Series module's soft front panel.

External Reference

Lock to 10MHz causes the ADC clock to lock to the 10 MHz reference connected to the 10 MHz I/O connector. **Free Run** allows internal oscillators to run at indeterminate frequencies. **PCI Backplane** (3030C/3035C/3036 only) causes the ADC clock to lock to the 10 MHz reference from the PCI backplane.

Input conditioning

RF Input Level (dBm)

Set this to the peak level of the input RF signal to insure the best dynamic range and signal-to-noise ratio.

Set the RF input level using the up/down arrows or by entering the level, in the range –99.00 to +30.00 dBm (+22 dBm, 3030A only) in Auto Atten Config mode. In Auto IF or Manual Atten Config mode, this value is not used but the maximum value is capped to +20 dBm.

IF Input Level (3030A/3035 only)

Set this to the peak level of the input signal to insure the best dynamic range and signal-to-noise ratio. Grayed out when Input Source is set to RF.

Set the IF input level using the up/down arrows or by entering the level, in the range –99.00 to +17.00 dBm for full scale on the digitizer.

Note: *the maximum safe input with 0 dB IF attenuation is +10 dBm.*

Step size: double-click on the step value under the IF Input Level field to set up the size of RF and IF level step.

RF Atten

Sets the RF attenuator value, which changes the input level to the mixer. This value can only be adjusted manually if Atten Config is set to Manual or Auto IF.

Set the RF attenuator level using the up/down arrows or by entering the level, in the range 0 to +31 dB, in 1 dB steps.

IF Atten

Sets the IF attenuator value, which changes the input level to the ADC. This value can only be adjusted manually if Atten Config is set to Manual.

Set the IF attenuator level using the up/down arrows or by entering the level in 1 dB steps (you are unlikely to use more than +31 dB).

Input Level Dimensions

Establishes the measurement units as dBm, dBµV, dBmV, dBV, V or mW.

Atten Config

Auto	the RF input level set is used to optimize RF and IF attenuator gain settings automatically.
Auto IF	you have manual control of RF attenuation and preamp but the IF attenuator setting is automatically set by the driver.
Manual	you have complete control over the settings of the RF and IF attenuators and preamp; the driver ignores the set RF input level.

Filter Bypass

When enabled, causes the anti-aliasing filter to be bypassed, allowing signals outside its passband to reach the ADC. Level calibration is maintained. Allows you to observe spurii and other signals within the module's bandwidth that would otherwise be removed by the filter.

ADC Overload (LED)

Indication is red if the ADC was overloaded during the last acquisition.

ADC Overload Level

Indicates the RF input level that could cause ADC Overload error. The displayed overload level is clamped to the safe input level.

Pre-Amp (3030C/3035C/3036 only)

When Atten Config is set to Auto IF or Manual, ticking this box switches in the preamp. In Auto mode, the preamp is switched in automatically when signal levels require it.

Remove DC Offset (3030C/3035C/3036 only)

Tick this box to remove the DC component from captured IF or IQ data. DC components at the edge of the span at full and/or ½ sample rate are removed.

***Note**: if no signal is present on the input, a sawtooth waveform is displayed on I and Q time series screens, due to a DC component introduced internally by the ADC transfer function.*

DC Offset (3030A/3035 only)

Click this button to control DC offset and dither:

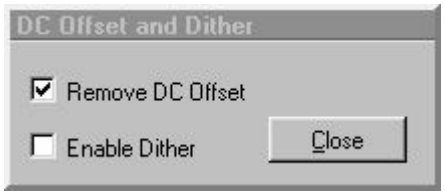


Fig. 9 DC offset and dither control

Remove DC Offset

Tick this box to remove the DC component from captured IF or IQ data. DC components at the edge of the span at full and/or ½ sample rate are removed.

DC offset removal is enabled by default.

***Note**: if no signal is present on the input, a sawtooth waveform is displayed on I and Q time series screens, due to a DC component introduced internally by the ADC transfer function.*

Enable Dither

Dither adds an uncorrelated noise-like signal that is outside the digitizer's normal operating bandwidth to the input of the ADC. This smooths out nonlinearities and helps to improve ADC noise floor, distortion products and level linearity. The dither element is removed when the signal is decimated and converted to IQ data; but to prevent interference with triggering, or if no decimation is used, there is also a dedicated digital dither filter.

Dither is off by default.

When dither is enabled, the dither filter is enabled by default.

This table shows how the DC offset removal and dither tick boxes interact:

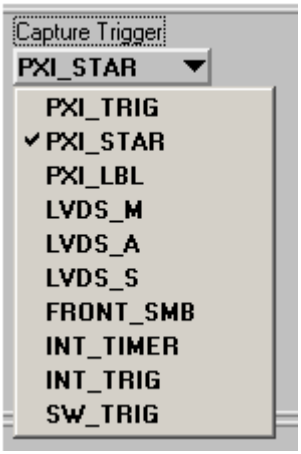
Remove DC Offset	Enable Dither not ticked	Enable Dither ticked
Ticked	DC offset tracked out	Dither removal filter is enabled DC offset is removed
Not ticked	DC offset is not removed	Dither removal filter is disabled DC offset is not removed

The waveform in Fig. 5 has dither enabled and DC offset removed.

Acquisition & triggering

Capture Trigger

Allows you to select the trigger source from a drop-down list:



Software trigger

- **SW_TRIG**
  This is a non-triggered capture mode. Click on **Start** to capture samples (defined by Number of Samples) when in Single/Repeat mode, without waiting for any external event. Click **Stop** to end the capture.

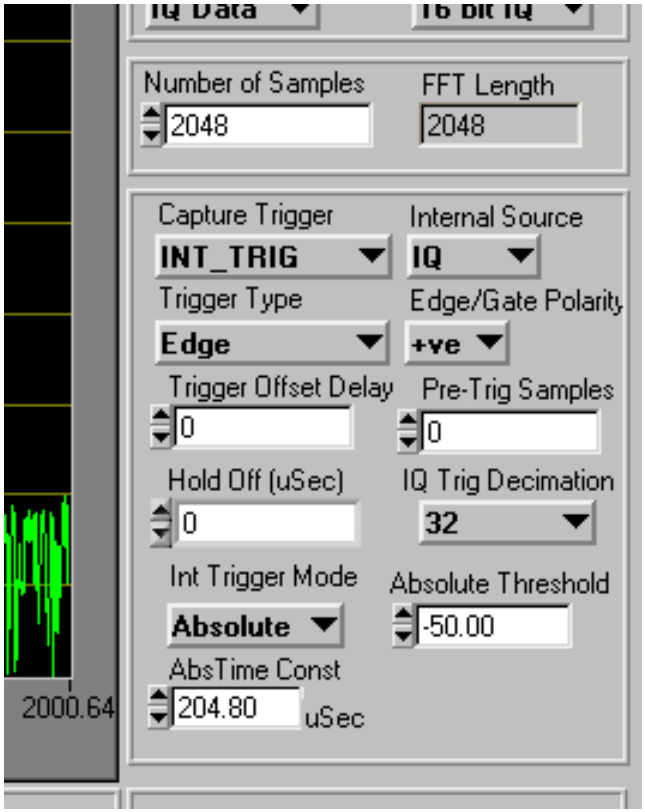
Hardware triggers

Remaining triggers on the drop-down list are hardware triggers. When any of these is selected, triggering is dependent on trigger events, including the correct arming of the trigger.

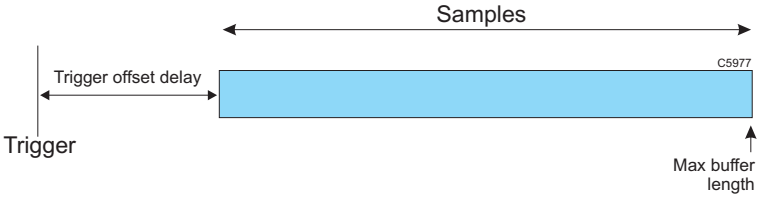
The module ignores triggers that occur during the sample capture.

Refer to the help files for full details.

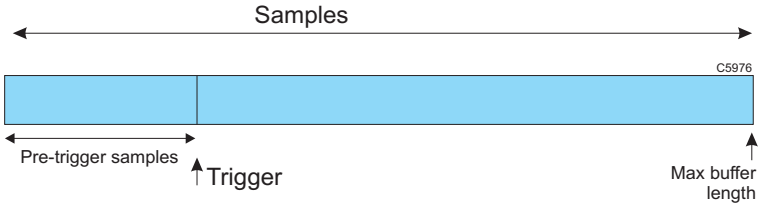
Most of the hardware triggers share a common triggering interface:



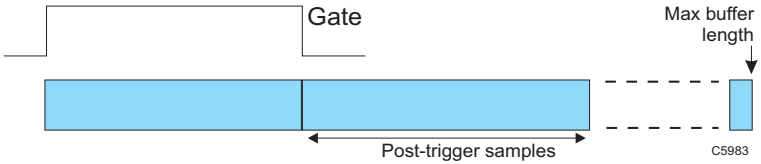
Internal Source	Set IQ or IF triggering. IQ triggering allows IQ selective triggering (3030C/3035C/3036 only).
Trigger Type	Set to Edge or Gate
Edge/Gate Polarity	Set +ve or –ve
Trigger Offset Delay	Delays the trigger by a specified number of output sample periods.



Pre-Trig Samples (Edge trigger type)	Sets the number of pre-trigger samples present in the captured data buffer. Increase this value to move the position of the trigger point in the captured data further from the start.

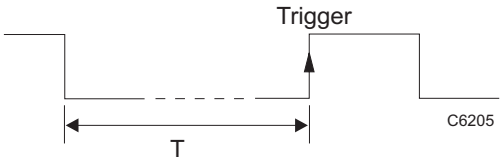


Post-Trig Samples (Gate trigger type)	Sets the number of post-trigger samples present in the captured data buffer.



Trigger Hold-Off

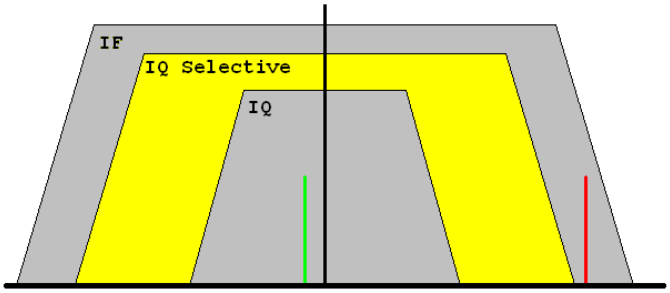
The trigger signal is valid only if the inactive period T before the active edge of the signal is greater than the specified trigger hold-off period.



IQ Trig Decimation

This function is enabled only when Internal Source is set to IQ.

The internal IF trigger is a broadband trigger with a bandwidth equal to the IF bandwidth of the digitizer. IQ trigger decimation allows you to further decimate the trigger signal so that the IQ trigger bandwidth (shown in yellow below) is reduced to near that of the captured signal. This avoids triggering on signals (shown in red below) that are outside the bandwidth of interest.



The range available is determined by the Decimation Ratio.

- **PXI_TRIG** [0–7]
  Takes its trigger input from any one of eight bits of the PXI trigger bus that is common to all modules in the chassis.

- **PXI_STAR**
  Takes its trigger input from a module that has ST functionality and is fitted in PXI slot 2.

- **PXI_LBL** (Local Bus Left) [6] (**3030C/3035C/3036 only**)
  Takes its trigger input from the slot to the left of the 3030C/3035C/3036 module (viewed from the front panel), using the PXI local bus. This bit is common only to the 3030C/3035C/3036 module and the module to its left.

- **PXI_LBL** (Local Bus Left) [0–12] (**3030A/3035 only)**
  Takes its trigger input from the slot to the left of the 3030A/3035 module (viewed from the front panel), using the PXI local bus. Choose from any of 13 bits for the trigger; this bus is common only to the 300A/3035 module and the module to its left.

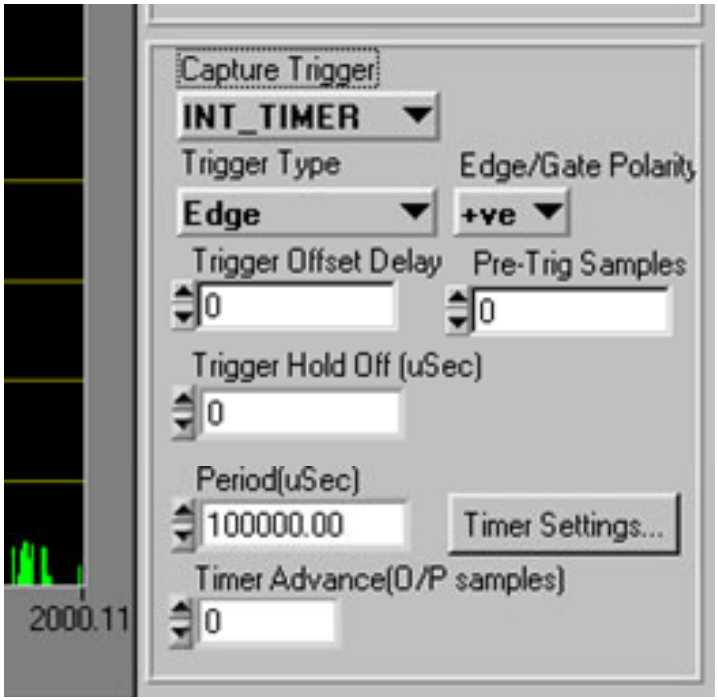
- **LVDS_M** [1–4]
  Takes its trigger from any of four Marker bits on the DATA connector. Ensure that Settings/LVDS/Marker Mode is set to Input.

- **LVDS_A** [0–4]
  Takes its trigger from any of five Auxiliary input bits on the DATA connector. Ensure that Settings/LVDS/Auxiliary Mode is set to Input.

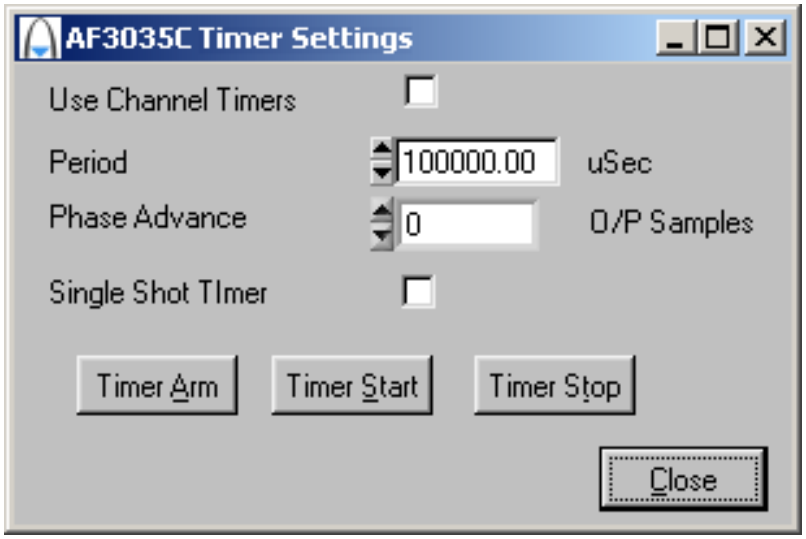
- **LVDS_S**
  Takes its trigger from the Spare 0 input bit on the LVDS data bus. Ensure that Settings/LVDS/Data Mode is set to Input. Because the data bus is set to receive when this trigger is used, it is not then possible to output data on the DATA connector.

- **FRONT_SMB**
  Takes its trigger from the TRIG connector on the module's front panel.

- **INT_TIMER**
  Takes its trigger from the internal timer. This timer trigger can also be routed to other modules using the routing matrix. Similarly, this timer can be synchronized with the external signal connected to the TIMER_SYNC signal in the routing matrix.



Click **Timer Settings…** to display the Timer Settings screen.



Use Channel Timers

When checked, lets you use a different timer period for each channel. The timer period is determined by the active channel's Period (see below), and applies while that channel is active. This mode is useful in setting up variable dwell list mode.

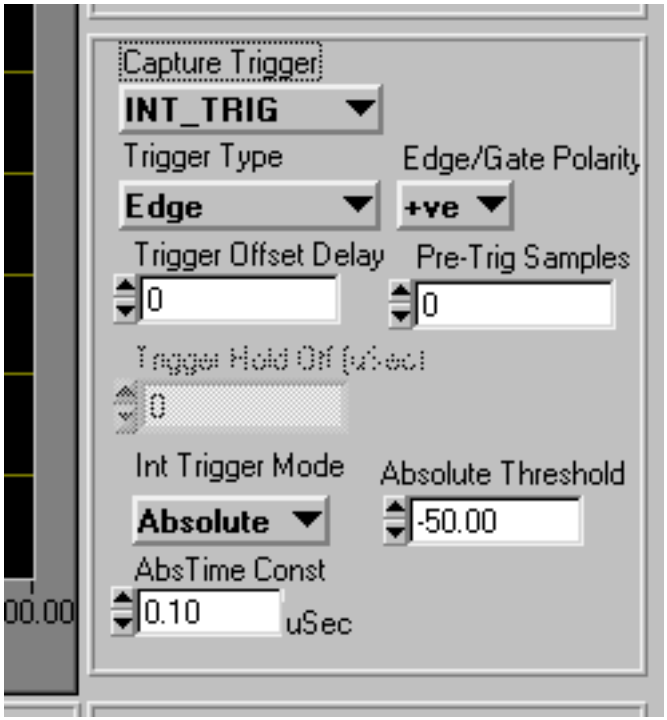
The channel timer period is measured in number of output samples, so changes if the sample rate changes. When the channel changes, the timer restarts, using the period set for that channel.

If Use Channel Timers is disabled, the timer period becomes the common timer period, specified in µs. This timer period stays the same irrespective of which channel is active, and does not restart when the channel changes.

Period	Sets the period of the active channel (in number of output samples) if Use Channel Timers is enabled. Otherwise, sets the common timer period in µs. Mark/space ratio in either mode is 50%.
Phase Advance	Adjusts the phase of the internal timer signal in multiples of the output sample clock period. Allows you to synchronize the timer trigger with an external signal. Not available if Use Channel Timers is enabled.
Single Shot Timer	Enables/disables the timer's single shot mode. When enabled, the timer stops after the timeout; otherwise, it runs continuously. Once the timer starts in single shot mode, subsequent triggers/starts are ignored until it stops (the timer cannot be retriggered while it is already running).
Timer Arm	Arms the timer so that an external signal connected to TIMER_TRIG in the routing matrix triggers the timer (rising edge).
Timer Start	Starts the timer if it was stopped, otherwise ignored if the timer is already running. Initial state of timer is ‘High’.
Timer Stop	Stops the timer if it is running, and disarms the timer trigger. Once the timer is stopped, an external signal cannot start it without re-arming it.

Settings for Period and Phase Advance (in common timer mode only) appear on the front panel as well as on the Timer Settings screen.

- **INT_TRIG**
  Takes its trigger from the internal level trigger.



Int Trigger Mode	Select the internal level trigger mode: Absolute/Relative Absolute: the digitized signal is filtered using an absolute time constant. An internal level trigger is generated when the level of this filtered signal exceeds the absolute level trigger threshold (specified in dBm). The absolute time constant and level settings may affect the trigger delay. Relative: the digitized signal is filtered using both a fast and a slow time constant. For a step level change, the amplitude difference between the two resultant filtered signals produces a pulse, its duration and level determined by the difference between the fast and slow time constants. The pulse is then compared with the 'relative threshold trigger level' to create the internal trigger. Fig. 10 shows this. When the relative threshold trigger level is entered as positive, the difference signal = (fast signal – slow signal). When relative threshold trigger level is entered as negative, the difference signal = (slow signal – fast signal). Only +ve Trigger Edge/Gate Polarity is available when using relative mode.
AbsTime Const	Sets the time constant for the absolute level internal trigger.
Absolute Threshold	Sets the absolute threshold level in dB.
Slow/Fast Time Const	Sets the slow and fast time constants used in relative internal trigger mode.

Relative Threshold — The threshold value (dB) compared with the difference signal filtered using Relative Slow and Fast Time Constants.

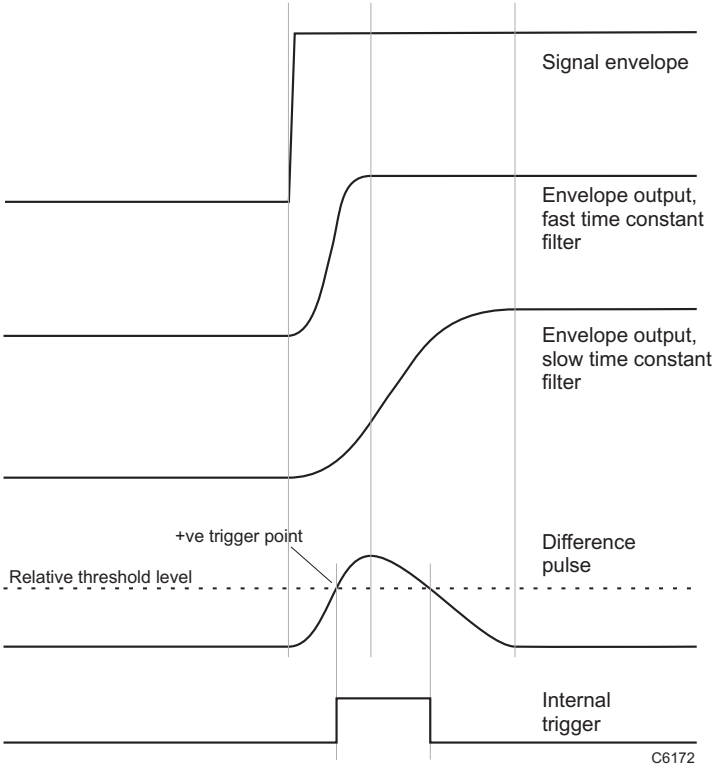


Fig. 10 Relative internal level trigger mode

Trigger mode and control

Mode:

Selects **Single**-shot or **Repeat** data capture.

Use with the **Start** and **Stop** buttons to initiate and stop data capture.

The indicator shows the status of the trigger or capture: green when waiting for a trigger or capturing, gray when idle.

IF/IQ data format

Sample Data Type

Select IQ or IF sample data type.

- IQ Sample Data: output sample rate is determined by the Modulation Mode and Decimation Ratio
- IF Sample Data: output sample rate is fixed at 250 MHz (3030C/3035C/3036) or 103.68 MHz (3030A/3035).

Modulation Mode

(IQ data format only) Sets the digital modulation mode. Select from Generic, UMTS, GSM, CDMA2000 1X or 2319 Emulation.

The sample rate varies, depending upon modulation mode and decimation ratio:

- Generic: user-defined. Use this mode to create or emulate any modulation scheme.

  3030C/3035C/3036 only:
  Enter any Undecimated Sample Rate in the range 7630 Hz to 250 MHz (PCI transfer) (90 MHz, 62.5 MHz, 31.25 MHz LVDS 16-bit IQ data transfer or 45 MHz, 31.25 MHz, 15.625 MHz 32-bit IQ data transfer — see LVDS Clock Rate) with a Generic Decimation Ratio of 1.

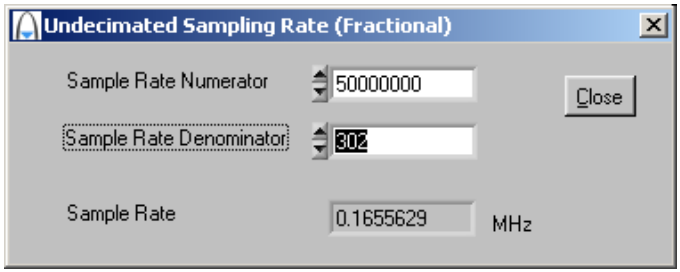
  3030A/3035 only:
  Enter any Undecimated Sample Rate in the range 6328.125 Hz to 85 MHz (PCI transfer) or 51.84 MHz (LVDS transfer) — see LVDS Clock Rate) with a Generic Decimation Ratio of 1.

Alternatively, enter a different Generic Decimation Ratio and scale the Undecimated Sample Rate accordingly.

The resultant sample rate is shown in the Decimated Sample Rate box.

or

define a fractional rate by setting the numerator and denominator. Click on the button adjoining the Undecimated Sample Rate box to open the popup panel and enter a fractional sample rate:



Pre-defined rates:

- UMTS data mode: 61.44 MHz/2^N (where N = 1 to 10)
- GSM resampled IQ data mode: 13 MHz/(3 * 2^N), where N = 0 to 4 ($2^{(4-N)}$ times symbol rate of 13 MHz/48)
- CDMA2000 1X resampled IQ data mode: 9.8304/2^N, where N = 0 to 3 ($2^{(3-N)}$ times chip rate of 1.2288 MHz)
- 2319 emulation mode: 65.28/2^N, where N = 4 or 5.

Decimation Ratio (Generic/GSM/UMTS/CDMA2000 X1/2319E)

(IQ data format only) Select a decimation ratio, dependent on the modulation mode:

GENERIC	2^n where n = 0 to 14 (max)
GSM	2^n where n = 0 to 4
UMTS	2^n where n = 1 to 10
CDMA2000 1X	2^n where n = 0 to 3
2319E emulation	2^n where n = 4, 5

See Data timing.

Undecimated Samp Rate (MHz)

Displays the internal undecimated sampling rate before division by the decimation ratio.

GENERIC	250 MHz	3030C/3035C/3036 only
	max. 85 MHz	3030A/3035 only
UMTS	61.44 MHz	= 3.84 MHz (3GPP chip rate) x 16
GSM	4.3333 (rec.) MHz	= 270.8333 (rec.) kHz (GSM bit rate) x 16
CDMA2000 1X	9.8304 MHz	= 1.2288 MHz (CDMA2000 chip rate) x 8
2319E	65.28 MHz	= 3.84 MHz (3GPP chip rate) x 17
IF	250 MHz	3030C/3035C/3036 only
	103.68 MHz	3030A/3035 only

IQ Data Output Format (3030C/3035C/3036 only)

Select 16- or 32-bit, subject to the modulation mode and decimation ratio chosen.

Sample rates

Modulation	Decimation ratio	IQ sample rate (Msymbol/s)	IQ data format
GENERIC	2n where n = 0 to 14 (max)	variable	6 (when Output Sample Rate > 31.25 MHz) 16/32 (when Output Sample Rate ≤ 31.25 MHz)
UMTS	2	30.72	16/32
	4	15.36	16/32
	8	7.68	16/32
	16	3.84	16/32
	32	1.92	16/32
	64	0.96	16/32
	128	0.48	16/32
	256	0.24	16/32
	512	0.12	16/32
	1024	0.06	16/32
GSM	1	4.33333	16/32
	2	2.16666	16/32
	4	1.08333	16/32
	8	0.541667	16/32
	16	0.270833	16/32
CDMA2000	1	9.8304	16/32
	2	4.9152	16/32
	4	2.4576	16/32
	8	1.2288	16/32
2319E	16	4.08	16/32
	32	2.04	16/32

IQ Data Output Format (3030A/3035 only)

Select 16- or 32-bit, subject to the modulation mode and decimation ratio chosen.

Sample rates

Modulation	Decimation ratio	IQ sample rate (Msymbol/s)	IQ data format
GENERIC	2^n where n = 0 to 14 (max)	variable	16 (when Output Sample Rate > 12.96 MHz) 16/32 (when Output Sample Rate <= 12.96 MHz)
UMTS	2	30.72	16
	4	15.36	16
	8	7.68	16/32
	16	3.84	16/32
	32	1.92	16/32
	64	0.96	16/32
	128	0.48	16/32
	256	0.24	16/32
	512	0.12	16/32
	1024	0.06	16/32
GSM	1	4.33333	16/32
	2	2.16666	16/32
	4	1.08333	16/32
	8	0.541667	16/32
	16	0.270833	16/32
CDMA2000	1	9.8304	16
	2	4.9152	16
	4	2.4576	16
	8	1.2288	16/32
2319E	16	4.08	16/32
	32	2.04	16/32

Decimated Samp Rate (MHz)

Displays the result of the undecimated sampling rate divided by the decimation ratio.

Number of (IF/IQ) Samples

The name of the field changes to reflect the sample type selected.

Sets the sample size (number of samples to be captured):

3030C/3035C/3036: up to 64 x 10^6 IQ pairs with 32-bit storage, 128 x 10^6 IQ pairs with 16-bit storage, or 256 x 10^6IF samples;
3030A/3035: up to 32 x 10^6 IQ pairs with 32-bit storage, 64 x 10^6 IQ pairs with 16-bit storage, or 128 x 10^6 IF samples.

FFT Length

Varies with number of IF/IQ samples set. Minimum 16, maximum 2048.

List mode operation

Introduction

List mode operation associates a list address with a particular RF setup (channels 0–127). When the module is set to list mode operation, a new address, when strobed in, causes the module to change to the RF setup (channel) associated with that address.

List mode operation facilitates fast channel hopping during, for example, testing of transmitter/receiver modules where numerous different RF level and frequency settings are needed. A seven-bit list address selects the channel. A strobe signal, internally or externally generated, then causes the instrument to switch between channels as required. Flexibility is provided to allow channel hopping using a variety of control sources.

List addresses for list mode operation can be provided manually, or from an external source via the signal routing matrix (providing access to backplane bus, LVDS and other address sources), or from an internal sequential counter. The strobe signal that changes the list address can be sourced externally via the routing matrix, or internally.

Channel List

Click **Chan List** on the soft front panel to display individual channel list settings (Fig. 11). This is where you define channel setup for list mode operation.

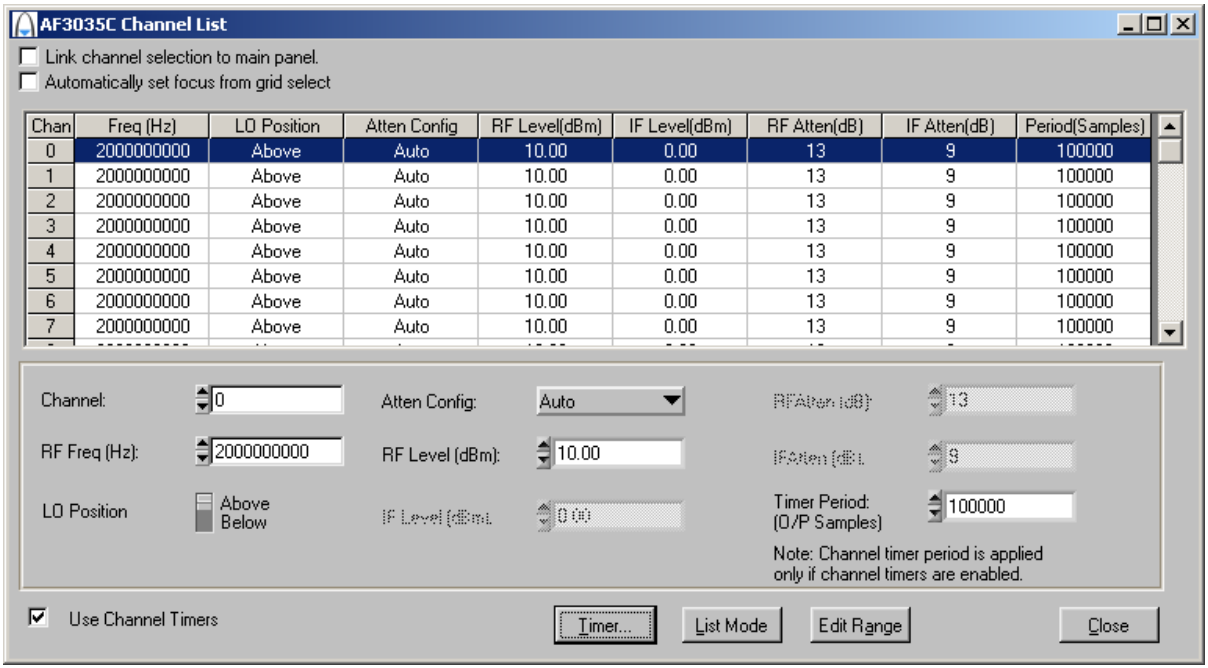


Fig. 11 Edit channel list settings (other 3030 Series are similar)

Edit individual channel parameters by selecting the specific channel. Channel parameters are:

- Freq (Hz)
- LO Position
- Atten Config
- RF Level (dBm)
- RF Atten (dB)
- IF Atten (dB)
- Period (µs/output samples)

Select the channel to be edited either by changing the channel number on the panel or by clicking on the corresponding channel row in the channel list.

If you check the **Link channel selection to main panel** box, changing the channel number on this panel makes it become the active channel on the soft front panel.

Check the **Automatically set focus from grid select** box to make the associated channel parameter field active when you click on a channel parameter in the grid.

Check the **Use Channel Timers** box to use the active channel's period as the timer period for that channel. If the box is unchecked, the common timer period (measured in µs) applies to all channels. See Timer Settings.

Click **Timer…** to display the Timer Settings screen.

Click **Edit Range** to display the Edit Channel Range screen (Fig. 12), which lets you apply changes to a set of channels simultaneously, speeding up channel setup.

Define start and finish values for address numbers in the **Chan range, from:** and **to:** fields.

Insert values and click **Set** for each field. You are asked to confirm each action. When finished, click **Close** to return to the Channel List screen.

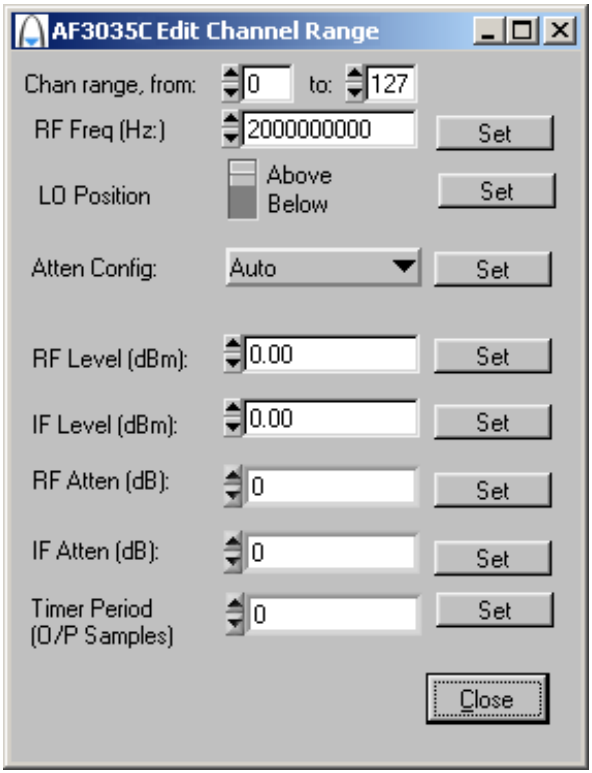


Fig. 12 Edit all channel settings (other 3030 Series are similar)

Click **List Mode** to display the List Mode Settings screen, which lets you set up addressing and strobing, and the internal counter.

List Mode Settings

Click **List Mode** on the Channel List screen to display the List Mode Settings screen. From here, you can define the list address source, and how the strobe (internal or external) that actions a new list address is handled. You can also set up the internal sequential counter and the timer that drives it.

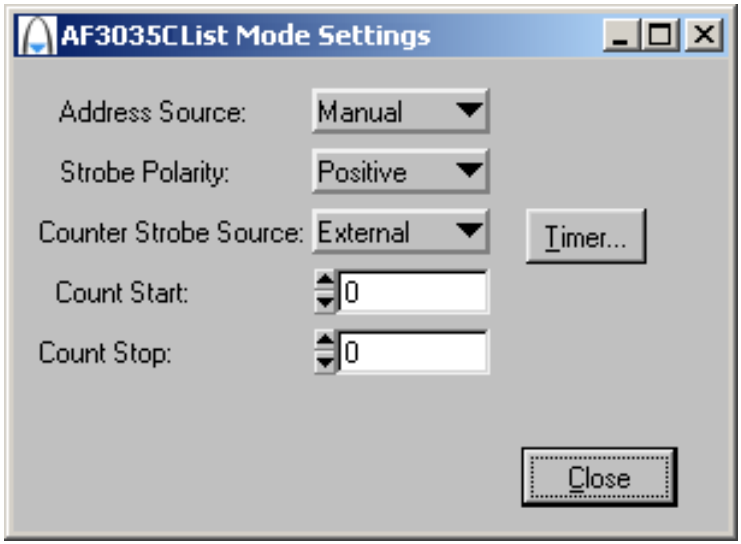


Fig. 13 Edit list mode settings (other 3030 Series are similar)

Address Source

Defines the source from which the seven-bit-wide list address is obtained.

Manual: RF list addresses are register-driven values, manually controlled by setting the **RF Channel**.

External: RF list addresses are sourced from the signal routing matrix (Fig. 7) on the strobe signal connected to LIST_STB.

Counter: RF list addresses are sourced from the internal sequential counter.

Strobe Polarity

Defines whether a positive- or negative-going edge is active for the strobe signal.

Counter Strobe Source

Defines the method used to sequence the internal List Counter register, when Address Source is set to Counter. When sequenced, the resulting change of address (the count value) automatically causes an internal strobe signal to be generated, which actions the new list address.

External: an external strobe, sourced from the signal routing matrix (Fig. 6), causes the counter to count up or down, providing a new list address.

Timer: the counter strobe signal is generated periodically by an internal timer, whose period is set by Timer Dwell.

Counter Start

Defines the start address of the list counter. If this value is less than the value of Counter Stop, the counter increments; otherwise it decrements. Setting this value also resets the list count to the next start address.

Counter Stop

Defines the stop address of the list counter. If this value is greater than the value of Counter Start, the counter increments; otherwise it decrements. Setting this value also resets the list count to the next start address.

Timer Dwell

Defines the period of the list timer, in units of 0.1 µs. The range is 1 µs to 600 s.

Timer...

Click to display the Timer Settings screen.

Program files

Program files are installed onto your computer from the CD-ROM.

Find registered com DLLs and ocx components, *.net* assemblies, libraries, source and associated help files in the program installation folder on your computer. This is typically:

C:\Program Files\Aeroflex\PXI

All executable C DLLs are installed in:

C:\WINDOWS\system32

Driver export functions

On-line help and functional documentation for driver export functions are available on the CD-ROM supplied with your module. They are installed onto your computer at the same time as the drivers.

Driver installation folder

Find help and functional documentation in the driver installation folder on your computer. If you did not change the default location, this is typically the same as for the VISA software.

Help

Within the driver installation folder are help files that provide detailed descriptions, parameter lists and return values for all available functions. Help files are provided in three formats:

af3030.doc	3030 Series function documentation	Text file
af3030.hlp	3030 Series Visual BASIC function reference	Windows® Help file format
af3030_C.hlp	3030 Series C language function reference	

We recommend that you use the C or Visual Basic formats, as these are easier to navigate.

The file opens at the Contents page:

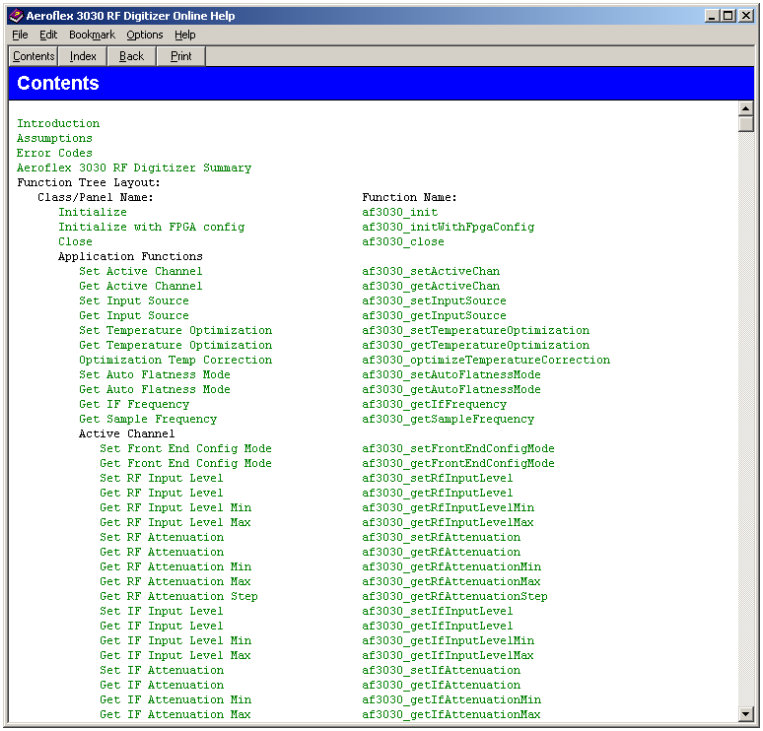


Fig. 14 Online help contents — example

Hyperlinks from here take you to

- Introduction
- Assumptions
- Error codes
- Functions listings

Functions listings

Functions are grouped by type. Click on the hyperlink for details of the function. Each function has a description of its purpose, and may have a list of parameters and return values.

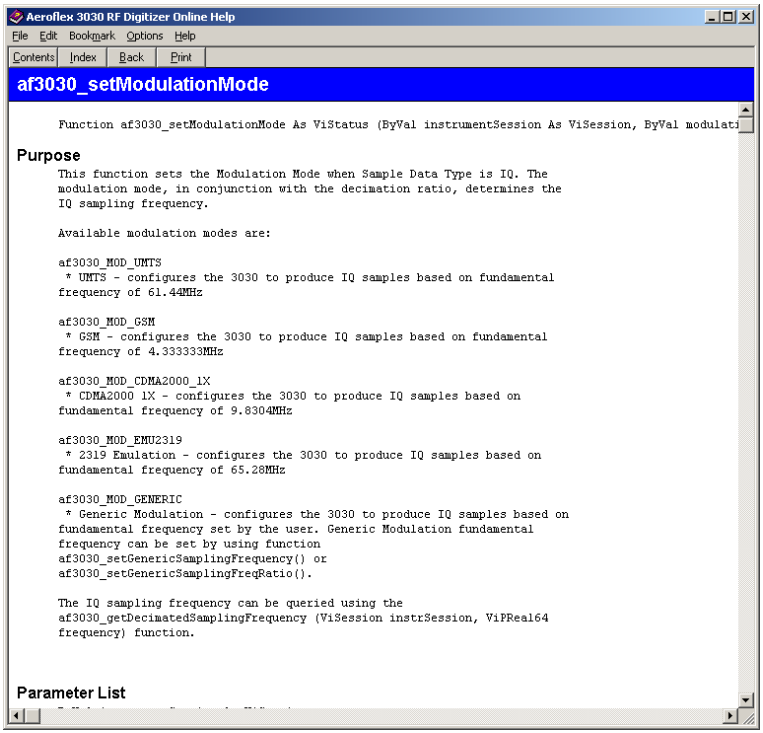


Fig. 15 Function description — example

RF digitizer using 3010 Series and 3030 Series

Refer to *3000 Series PXI Modules Installation Guide for Chassis* (part no. 46882/667) and *PXI Studio 2 User Guide* (part no. 46892/809), both supplied on the CD-ROM with the module, for detailed information on creating a fully functional RF digitizer, using a 3030 Series module and 3010 Series RF Synthesizer together. The afDigitizer dlls and PXI Studio 2 application combine the functions of the individual modules to provide a single interface with the appearance and functionality of an integrated instrument.

DATA connector and timing

The DATA connector is a 68-way female VHDCI-type LVDS (low-voltage differential signaling) interface. It can be used to output data and associated control and timing signals.

The DATA connector is shown in Fig. 16. LVDS data conforms to ANSI/TIA/EIA-644.

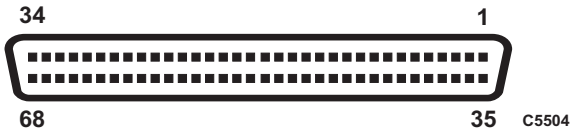


Fig. 16 DATA connector (looking onto front panel)

The DATA interface provides:

- output of IF or IQ data
- input/output of triggering, List Mode and Timer signals.
- clock.

The electrical level is LVDS: V_{OH} typically 1.38 V, V_{OL} typically 1.03 V

Table 1 DATA pin-out

Contact	Function	Contact	Function
1	AUX0-	35	AUX0+
2	AUX1–	36	AUX1+
3	AUX2–	37	AUX2+
4	SPARE1–	38	SPARE1+
5	SPARE2–	39	SPARE2+
6	CLK_IN–	40	CLK_IN+
7	GND	41	GND
8	CLK_OUT–	42	CLK_OUT+
9	D0–	43	D0+
10	D1–	44	D1+
11	D2–	45	D2+
12	D3–	46	D3+
13	D4–	47	D4+
14	D5–	48	D5+
15	D6–	49	D6+
16	D7–	50	D7+
17	D8–	51	D8+
18	D9–	52	D9+
19	D10–	53	D10+
20	D11–	54	D11+
21	D12–	55	D12+
22	D13–	56	D13+
23	D14–	57	D14+
24	D15–	58	D15+
25	IQSELECT_OUT–	59	IQSELECT_OUT+
26	IQSELECT_IN–	60	I/QSELECT_IN+
27	SPARE0–	61	SPARE0+

Contact	Function	Contact	Function
28	GND	62	GND
29	MARKER1–	63	MARKER1+
30	MARKER2–	64	MARKER2+
31	MARKER3–	65	MARKER3+
32	MARKER4–	66	MARKER4+
33	AUX3–	67	AUX3+
34	AUX4–	68	AUX4+

Data format (3030C/3035C/3036 only)

The data output to the DATA interface is real-time. In resample mode, data is output using a 180 MHz, 125 MHz or 62.5 MHz clock (depending on LVDS clock rate). The data is bursted to achieve the correct average sample rate.

D0-D15 (Sample DATA) in Output Mode	Sample Data Output Format: 16-bit IQ: 2 x D[15:0], I followed by Q, D[0]=LSB. 32-bit IQ: 4 x D[15:0] in order I MSW, I LSW, Q MSW, Q LSW, D[0]=LSB.
IQSELECT_OUT	Specifies content of D0-D15 in output mode when sample data format is IQ. IQSELECT=1 for rising CLK_OUT indicated I data on D0-D15. First IQSELECT transition to '0' from '1' on the rising edge of CLK_OUT indicates **start** of the Q data. In 16-bit mode, Q data is valid for one clock whereas in 32-bit mode, Q data is valid for two clocks after IQSELECT changes to 0. Note that IQSELECT stays 0 even if Q data is transferred. Thereafter, Q is indeterminate until IQSELECT_OUT goes positive to define a new IQ pair. IQSELECT_OUT stays =0 at all times in IF mode.
CLK_OUT	Output clock signal.

Data format (3030A/3035 only)

The data output to the DATA interface is real-time. In resample mode, data is output using a 103.68 MHz clock. The data is bursted to achieve the correct average sample rate.

D0-D15 (Sample DATA) in Output Mode	Sample Data Output Format: 16-bit IQ: 2 x D[15:0], I followed by Q, D[0]=LSB. 32-bit IQ: 4 x D[15:0] in order I MSW, I LSW, Q MSW, Q LSW, D[0]=LSB. IF data: there are two configurations: Upper 14 bits: D[15:2], D[2]=LSB (default mode) Lower 14 bits: D[13:0], D[0] = LSB, D[15:14] sign extended from D[13].
IQSELECT_OUT	Specifies content of D0-D15 in output mode when sample data format is IQ. IQSELECT=1 for rising CLK_OUT indicated I data on D0-D15. First IQSELECT transition to '0' from '1' on the rising edge of CLK_OUT indicates **start** of the Q data. In 16-bit mode, Q data is valid for one clock whereas in 32-bit mode, Q data is valid for two clocks after IQSELECT changes to 0. Note that IQSELECT stays 0 even if Q data is transferred. Thereafter, Q is indeterminate until IQSELECT_OUT goes positive to define a new IQ pair. IQSELECT_OUT stays =0 at all times in IF mode.
CLK_OUT	Output clock signal.

Data timing

Data transmission for generic modulation mode

3030C/3035C/3036 only

In this mode, IQ data is resampled to produce IQ data in the range 180 MHz/2^N, 125 MHz/2^N or 62.5 MHz/2^N, where N = 1 to 14. The clock frequency depends on the LVDS Clock Rate setting. Example timing relationships between data rate and clock frequency for the DATA interface are shown in Fig. 17 and Fig. 18. These show a clock rate of 125 MHz, which is the default.

IQSEL_OUT is toggled only when an IQ data pair is being transmitted. Maximum IQ sample rate is 90 Ms/s (for 16-bit I&Q) or 45 Ms/s (for 32-bit I&Q). In Fig. 17, it is a non-integer value, and only the Q value occupying the clock period that follows the falling edge of IQSEL_OUT is valid. In Fig. 18, the chosen decimated data rate of 62.5 Ms/s means that the ratio of clock to data rate is 2.

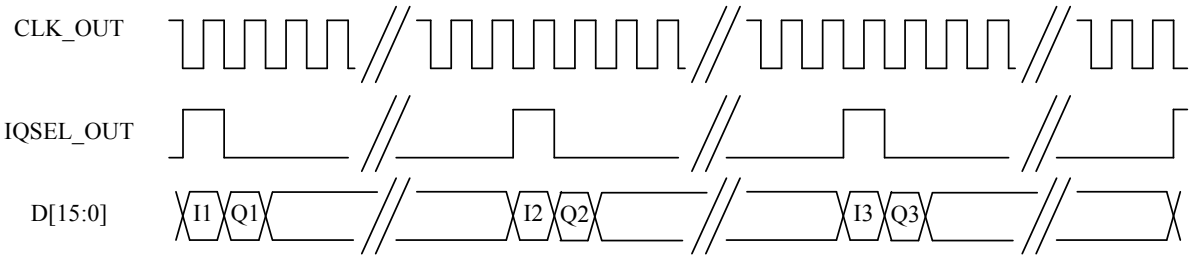


Fig. 17 DATA timing for generic modulation in 16-bit IQ mode, non-integer relationship, 125 MHz clock

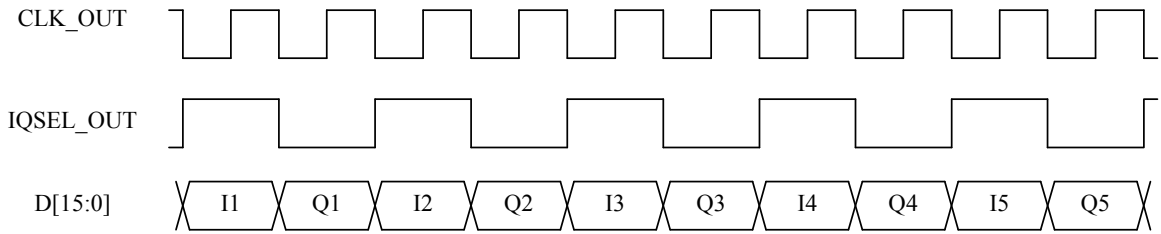


Fig. 18 DATA timing for generic modulation in 16-bit IQ mode, integer relationship, 125 MHz clock

3030A/3035 only

In this mode, IQ data is resampled to produce IQ data in the range 51.84 MHz/2^N, where N = 0 to 13. Example timing relationships between data rate and clock frequency for the DATA interface are shown in Fig. 19 and Fig. 20. IQSEL_OUT is toggled only when an IQ data pair is being transmitted. Note that the CLK_OUT signal is continuous and that the frequency of the clock remains fixed at 103.68 MHz. In Fig. 19, the chosen decimated data rate of 51.84 Ms/s means that the ratio of clock to data rate is 2. In Fig. 20, it is a non-integer value, and only the Q value occupying the clock period that follows the falling edge of IQSEL_OUT is valid.

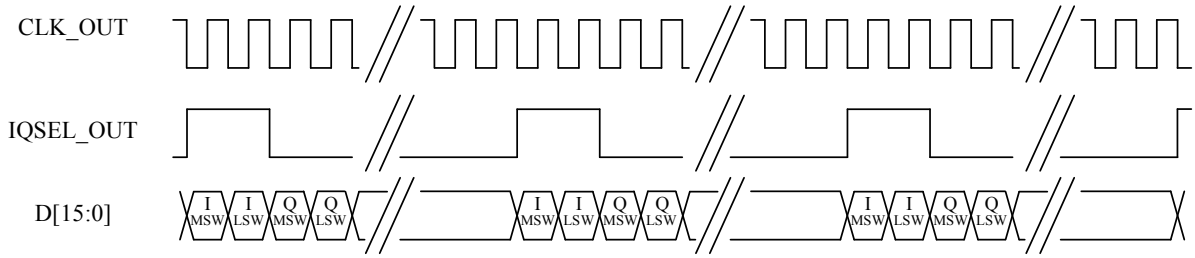


Fig. 19 DATA timing for generic modulation in 32-bit IQ mode, integer relationship

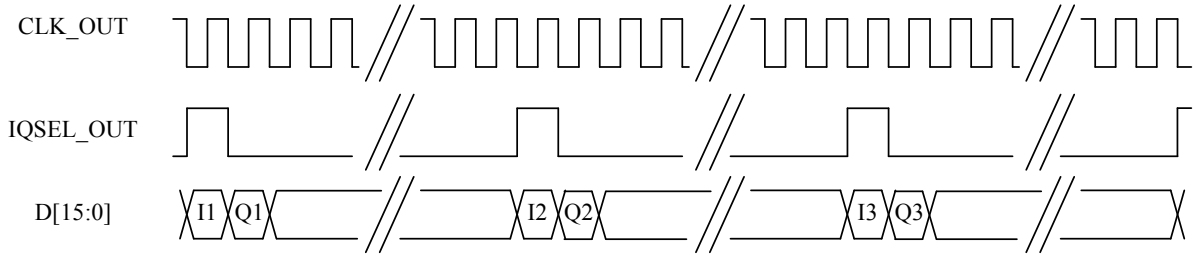


Fig. 20 DATA timing for generic modulation in 16-bit IQ mode, non-integer relationship

Data timing for UMTS modulation mode and decimation ratio of 2

3030C/3035C/3036 only

The LVDS clock rate is selectable between 180 MHz, 125 MHz or 62.5 MHz. The default is 125 MHz. The module's soft front panel allows the clock rate, the modulation mode and the decimation ratio to be selected. IQSELECT_OUT is toggled only when an IQ data pair is being transmitted. If UMTS is selected as the modulation mode and a decimation rate of two is selected, the IQ data rate is 30.72 Ms/s. The ratio of clock rate to IQ sample rate is (using default clock rate) $\frac{125\,\text{MHz}}{30.72\,\text{MHz}} = 4.07$, a non-integer value that means that data is output sometimes on the 4^{th} clock pulse and sometimes on the 5^{th}. Therefore the number of clock cycles between IQSELECT_OUT being asserted varies. When configured in this way, the timing relationships for the DATA interface are as shown in Fig. 21.

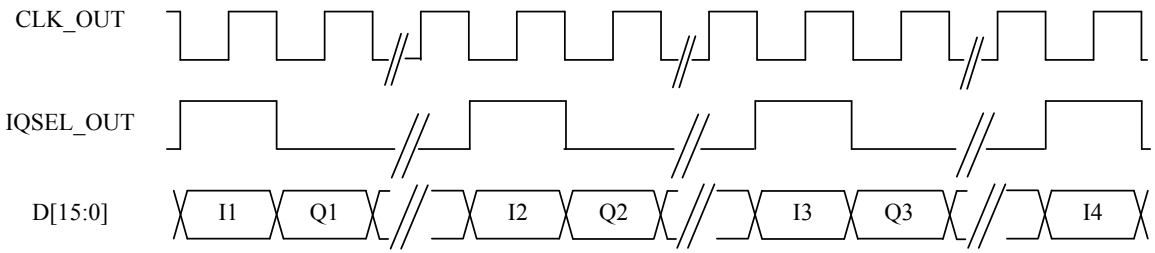


Fig. 21 DATA timing for UMTS mode and decimate by 2 for 16-bit IQ, 125 MHz clock

3030A/3035 only

The ADC in the module is clocked at a rate of 103.68 Ms/s. The module's soft front panel allows both the modulation mode and the decimation ratio to be selected. IQSELECT_OUT is toggled only when an IQ data pair is being transmitted. If UMTS is selected as the modulation mode and a decimation rate of two is selected, the IQ data rate is 30.72 Ms/s. The ratio of ADC clock rate to IQ sample rate is $\frac{103.68\,\text{MHz}}{30.72\,\text{MHz}} = 3.375$, a non-integer value that means that data is output sometimes on the 3rd clock pulse and sometimes on the 4th. Therefore the number of clock cycles between IQSELECT_OUT being asserted varies. When configured in this way, the timing relationships for the DATA interface are as shown in Fig. 22.

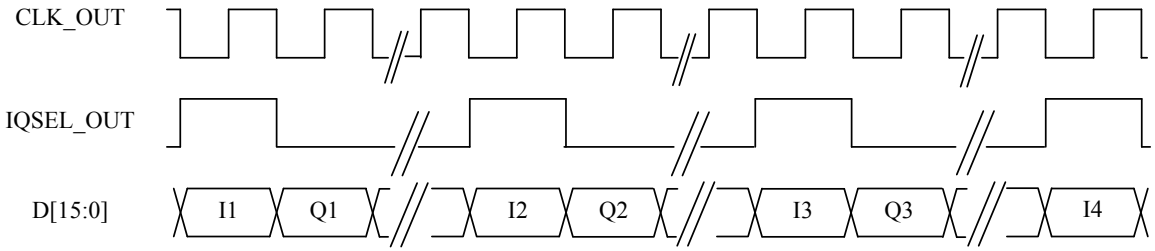


Fig. 22 DATA timing for UMTS mode and decimate by 2 for 16-bit IQ

Data timing for UMTS modulation mode and decimation ratio of 4

3030C/3035C/3036 only

An example of timing relationships for the DATA interface is shown in Fig. 23. The CLK_OUT signal is continuous and remains fixed, irrespective of the modulation mode and the decimation rate. The default is 125 MHz. The ratio of clock rate to IQ sample rate is (using default clock rate) $\frac{125\,\text{MHz}}{15.36\,\text{MHz}} = 8.14$, a non-integer value that means that data is output sometimes on the 8^{th} clock pulse and sometimes on the 9^{th}. Therefore the number of clock cycles between IQSELECT_OUT being asserted varies. IQSELECT_OUT is toggled only when an IQ data pair is being transmitted.

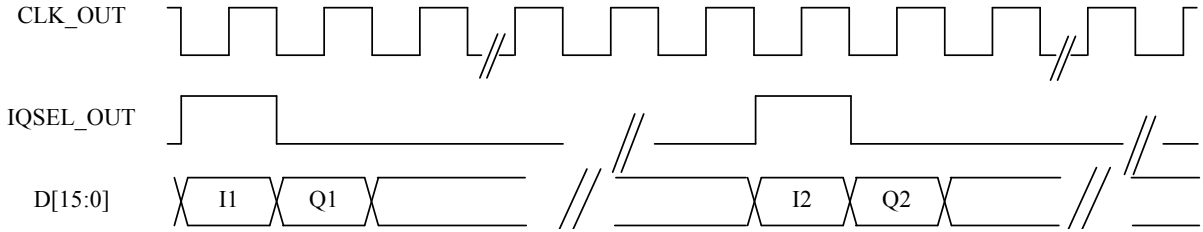


Fig. 23 DATA timing for UMTS mode and decimate by 4 for 16-bit IQ, 125 MHz clock

3030A/3035 only

The timing relationships for the DATA interface are as shown in Fig. 24. The CLK_OUT signal is continuous and remains fixed at 103.68 MHz, irrespective of the modulation mode and the decimation rate. The ratio of ADC clock rate to IQ sample rate is $\frac{103.68\,\text{MHz}}{15.36\,\text{MHz}} = 6.75$, a non-integer value that means that data is output sometimes on the 6^{th} clock pulse and sometimes on the 7^{th}. Therefore the number of clock cycles between IQSELECT_OUT being asserted varies. IQSELECT_OUT is toggled only when an IQ data pair is being transmitted.

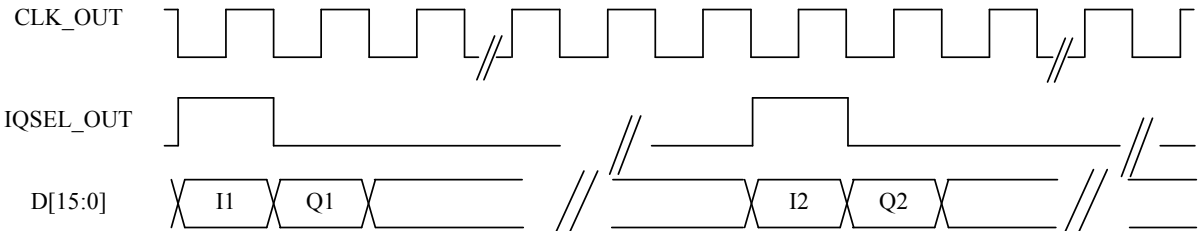


Fig. 24 DATA timing for UMTS mode and decimate by 4 for 16-bit IQ

Data timing for UMTS modulation mode and decimation ratio of 8

3030C/3035C/3036 only

An example of timing relationships for the DATA interface is shown in Fig. 25. The CLK_OUT signal is continuous and remains fixed at the selected LVDS clock rate, irrespective of the modulation mode and the decimation rate. The default is 125 MHz. The ratio of clock rate to IQ sample rate is (using default clock rate) $\frac{125\,\text{MHz}}{7.68\,\text{MHz}} = 16.28$. Therefore the number of clock cycles between IQSELECT_OUT being asserted varies. IQSELECT_OUT is toggled only when an IQ data pair is being transmitted.

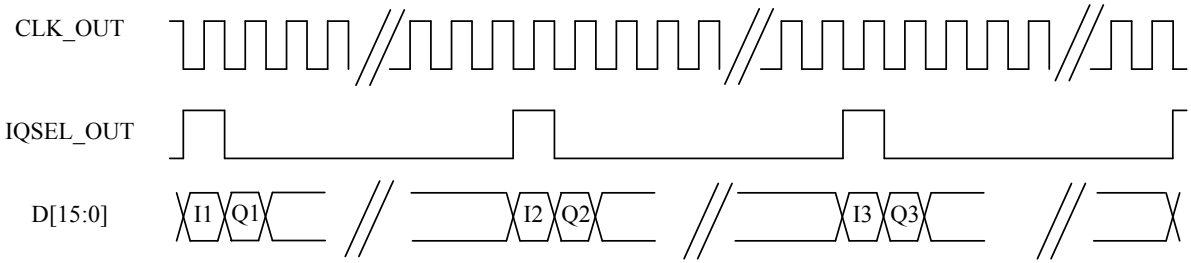


Fig. 25 DATA timing for 16-bit IQ UMTS mode and decimate by 8, 125 MHz clock

In 32-bit mode, data is transmitted as two 16-bit words, MSW then LSW for I then Q, as shown in Fig. 26.

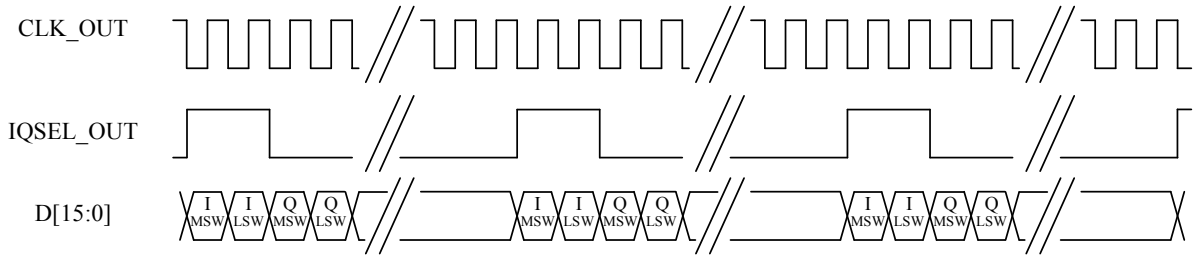


Fig. 26 DATA timing for 32 bit IQ, UMTS mode and decimate by 8

3030A/3035 only

The timing relationships for the DATA interface are as shown in Fig. 27. The CLK_OUT signal is continuous and remains fixed at 103.68 MHz, irrespective of the modulation mode and the decimation rate. The ratio of ADC clock rate to IQ sample rate is $\frac{103.68\,\text{MHz}}{7.68\,\text{MHz}} = 13.5$. Therefore the number of clock cycles between IQSELECT_OUT being asserted varies. IQSELECT_OUT is toggled only when an IQ data pair is being transmitted.

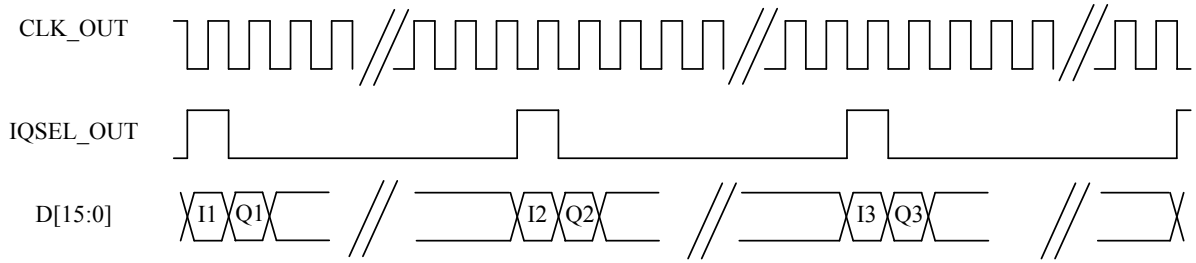


Fig. 27 DATA timing for 16-bit IQ UMTS mode and decimate by 8

In addition, for decimation ratios of 8 or greater, IQ data can be 32-bit. In this mode data is transmitted as two 16-bit words, MSW then LSW for I then Q, as shown in Fig. 28.

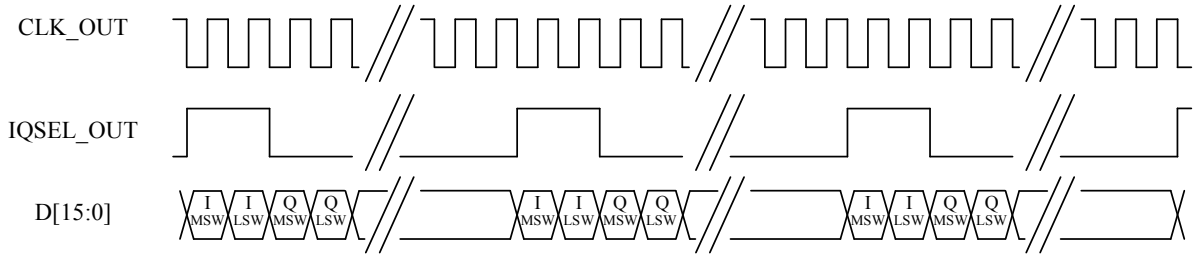


Fig. 28 DATA timing for 32 bit IQ, UMTS mode and decimate by 8

Data timing for CDMA2000 1X modulation mode

If a modulation mode of CDMA2000 1X and a decimation value of 1 are both selected, IQ data is generated at eight times the CDMA2000 1X chip rate. As the chip rate is 1.2288 MHz, this gives an IQ sample rate of 9.8304 Ms/s. There is no longer an integer relationship between the default clock rate of 125 MHz (3030C/3035C/3036) or 103.68 MHz (3030A/3035) and the 9.8304 Ms/s data rate in the example.

The number of clock cycles between IQSELECT_OUT being asserted is not fixed but varies. This is true for all CDMA mode decimation ratios.

An example of timing relationships for the DATA interface is shown in Fig. 29. Note that the CLK_OUT signal is continuous and remains fixed at the selected LVDS clock rate, irrespective of the modulation mode and the decimation rate. IQSELECT_OUT is toggled only when an IQ data pair is being transmitted.

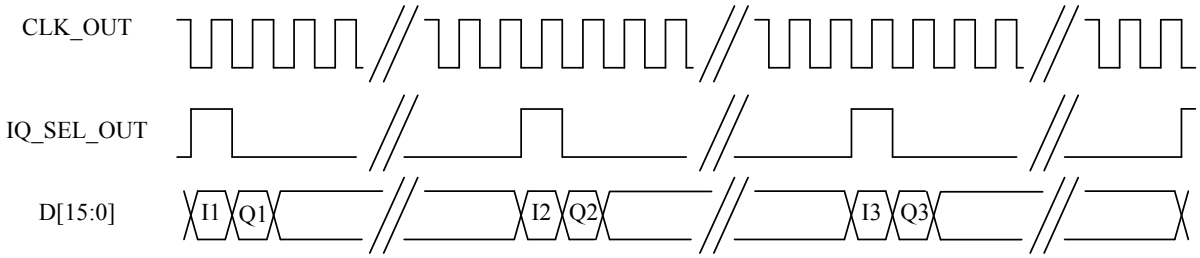


Fig. 29 DATA timing for CDMA2000 1X, 125 MHz clock

Data transmission for GSM modulation mode and a decimation ratio of 1

In this mode the IQ data is resampled to produce IQ data at 16 times the GSM symbol rate of 270.83 kHz, that is, 4.333 Ms/s. An example of timing relationships for the DATA interface is shown in Fig. 30. Note that the CLK_OUT signal is continuous and that the frequency of the clock remains fixed at the selected LVDS clock rate. IQSELECT_OUT is toggled only when an IQ data pair is being transmitted.

There is no integer relationship between the data rate of 4.33 MHz and the default clock frequency of 125 MHz (3030C/3035C/3036) or 103.68 MHz (3030A/3035) in the example. Therefore the number of clock cycles between IQSELECT_OUT being asserted is no longer fixed but varies. This is true for all GSM mode decimation ratios.

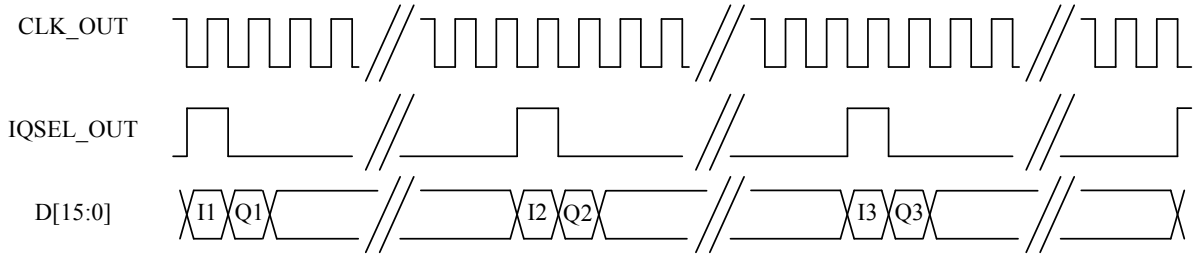


Fig. 30 DATA timing for GSM for 16-bit IQ, 125 MHz clock

Data transmission for 2319E emulation mode

In this mode, the IQ data is resampled to produce IQ data at 4.08 MHz with a decimation ratio of 16. An example of timing relationships for the DATA interface is shown in Fig. 31. Note that the CLK_OUT signal is continuous and remains fixed at the selected LVDS clock rate. IQSELECT_OUT is toggled only when an IQ data pair is being transmitted.

There is no integer relationship between the data rate of 4.08 MHz and the default clock frequency of 125 MHz (3030C/3035C/3036) or 103.68 MHz (3030A/3035). Therefore the number of clock cycles between IQSELECT_OUT being asserted is no longer fixed but varies. This is true for all 2319E modulation mode decimation ratios.

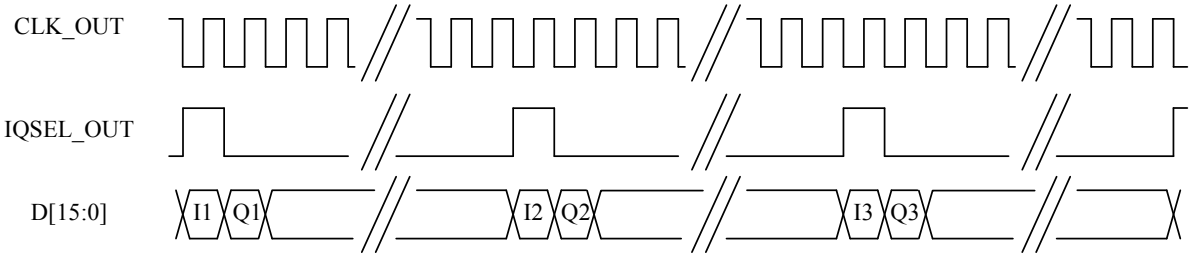


Fig. 31 DATA timing for 2319 emulation for 16-bit IQ, 125 MHz clock

BRIEF TECHNICAL DESCRIPTION

Introduction

A 3030 Series module is a PXI RF bandpass digitizer, digitizing an instantaneous IF bandwidth of 90 MHz (3030C/3035C/3036) or 36 MHz (3030A/3035). Digitized RF can be stored in a large internal RAM and read back over the PXI bus. It can also be streamed out of a front panel LVDS in the form of digital IQ samples.

Flexible signal and trigger processing is available. A 3030 Series module can be operated as a spectrum analyzer, modulation analyzer, demodulator or part of a radio test set, by selecting the appropriate application software.

A 3030 Series module comprises three printed circuit boards (four, 3035C/3036 only), occupying two or three slots in the backplane. It must be used with an external local oscillator (LO) from a 3010 Series RF synthesizer module or other RF source.

The first board is a single stage RF downconverter to IF, with an input attenuator and output gain. The IF output is normally linked externally to the second board, which digitizes the input IF signal. It has switchable input gain, an anti-alias filter with bypass and a clock source. It outputs data to the third board, which provides all of the digital services required by the module, including the power supply, PXI interface, LVDS interface, memory and digital signal processing.

3035C/3036 only

RF conversion to IF is achieved using two RF boards. The RF input signal is connected to the first of these two boards and then it is switched and routed depending upon the RF input frequency specified by the user.

Fig. 32 to Fig. 36 show block schematics for each module type.

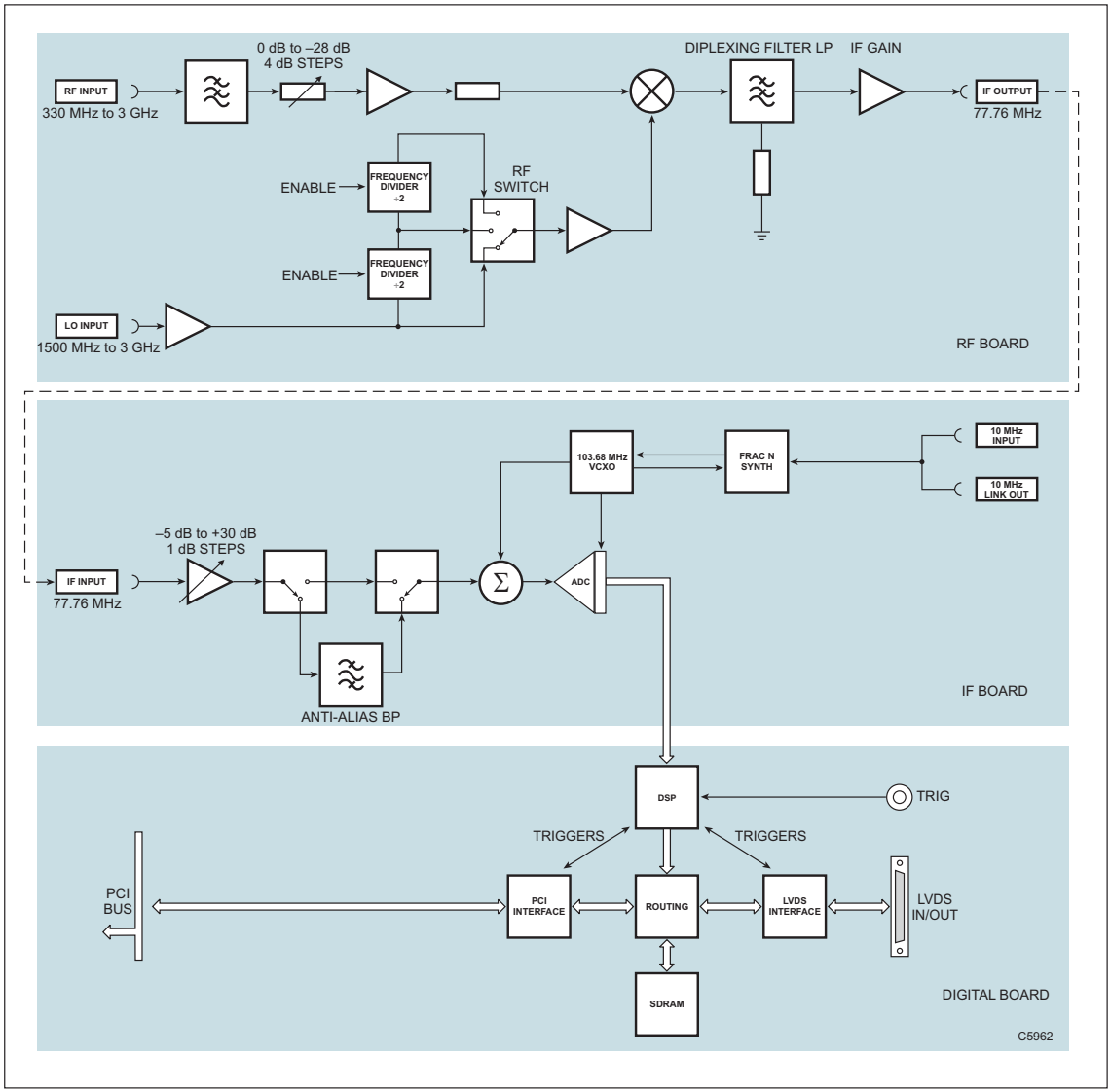


Fig. 32 3030A block schematic diagram

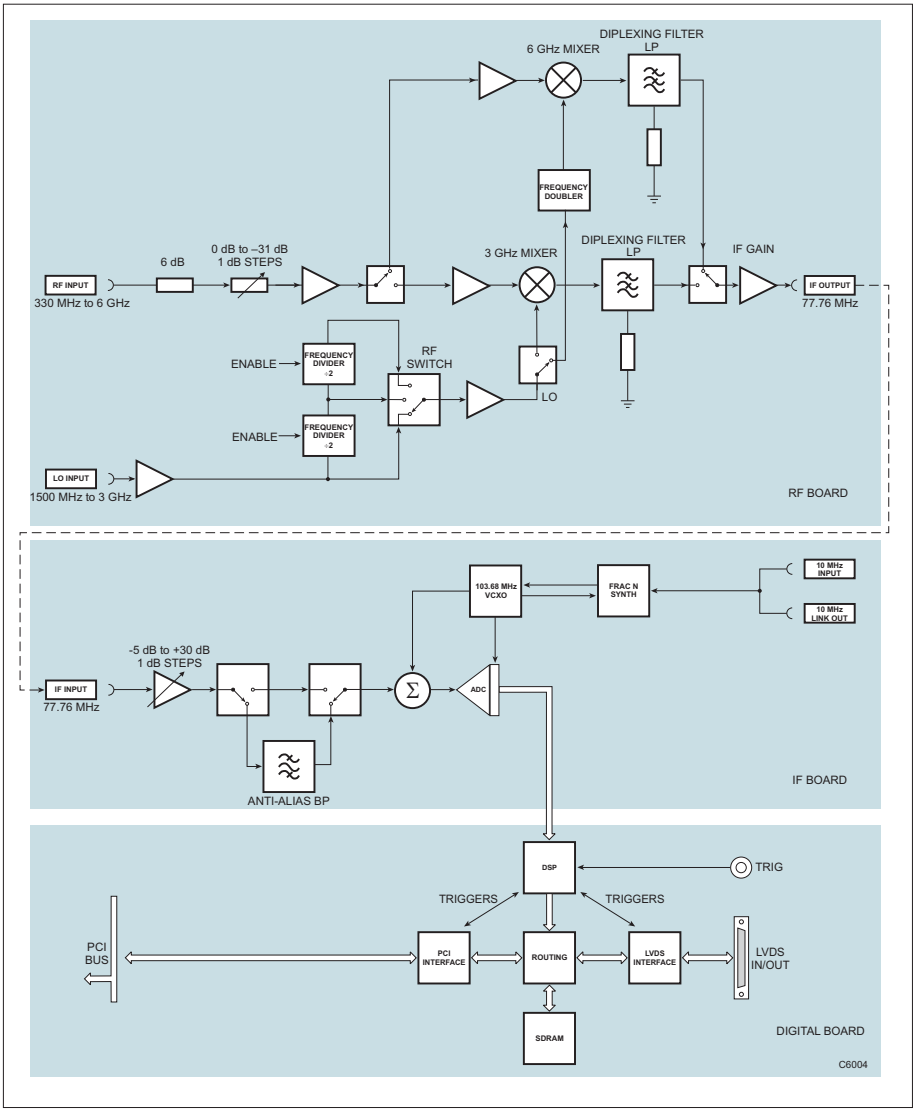


Fig. 33 3035 block schematic diagram

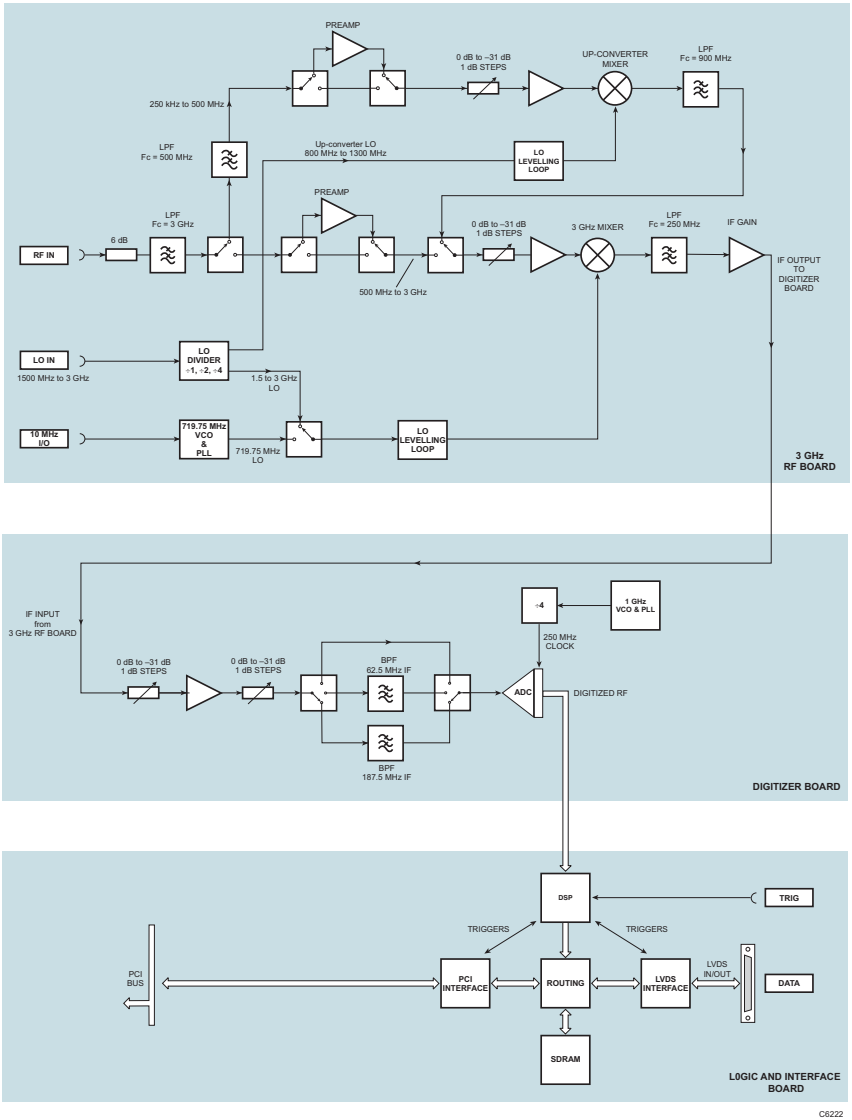
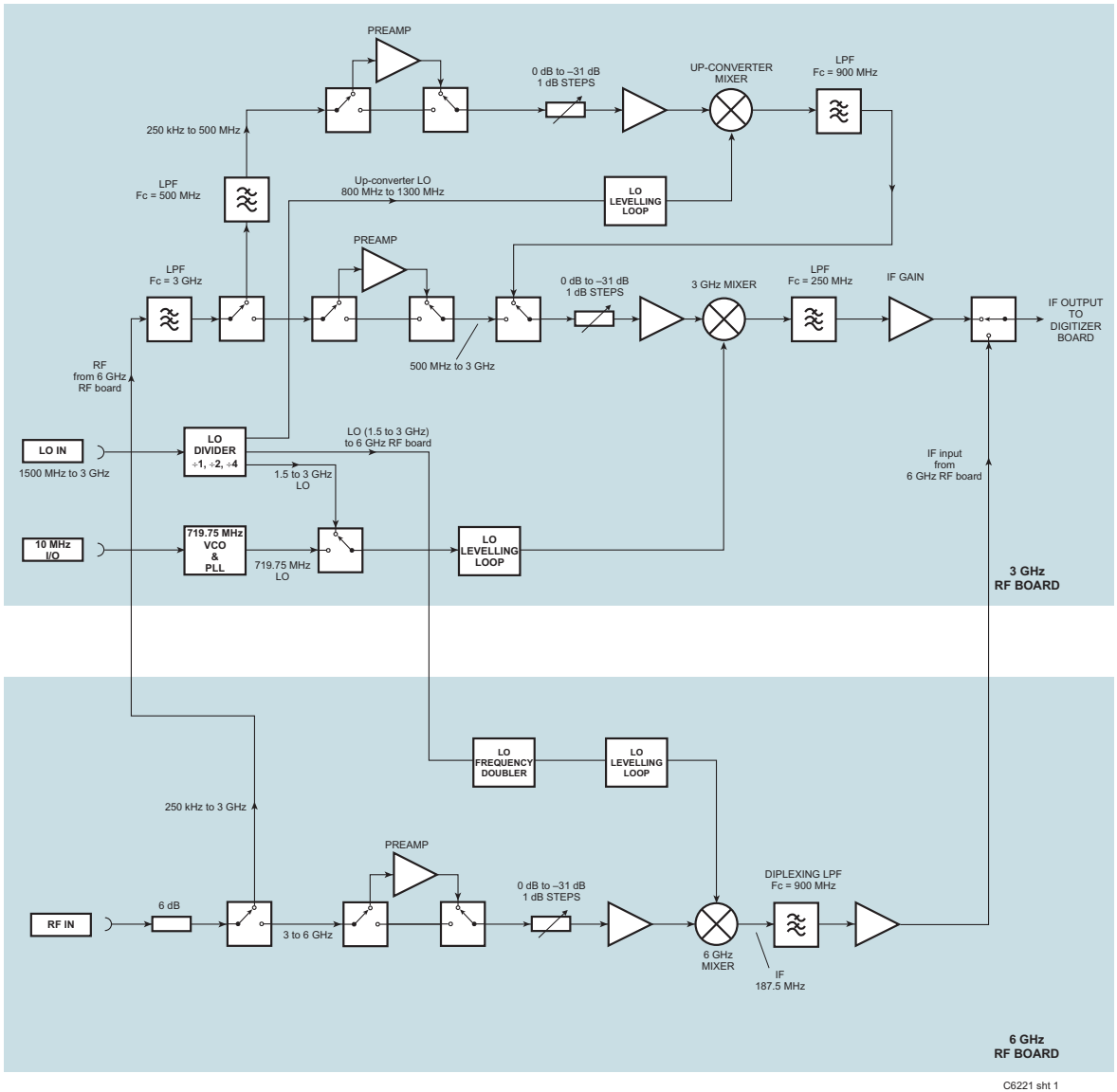


Fig. 34 3030C block schematic diagram



C6221 sht 1

continued…

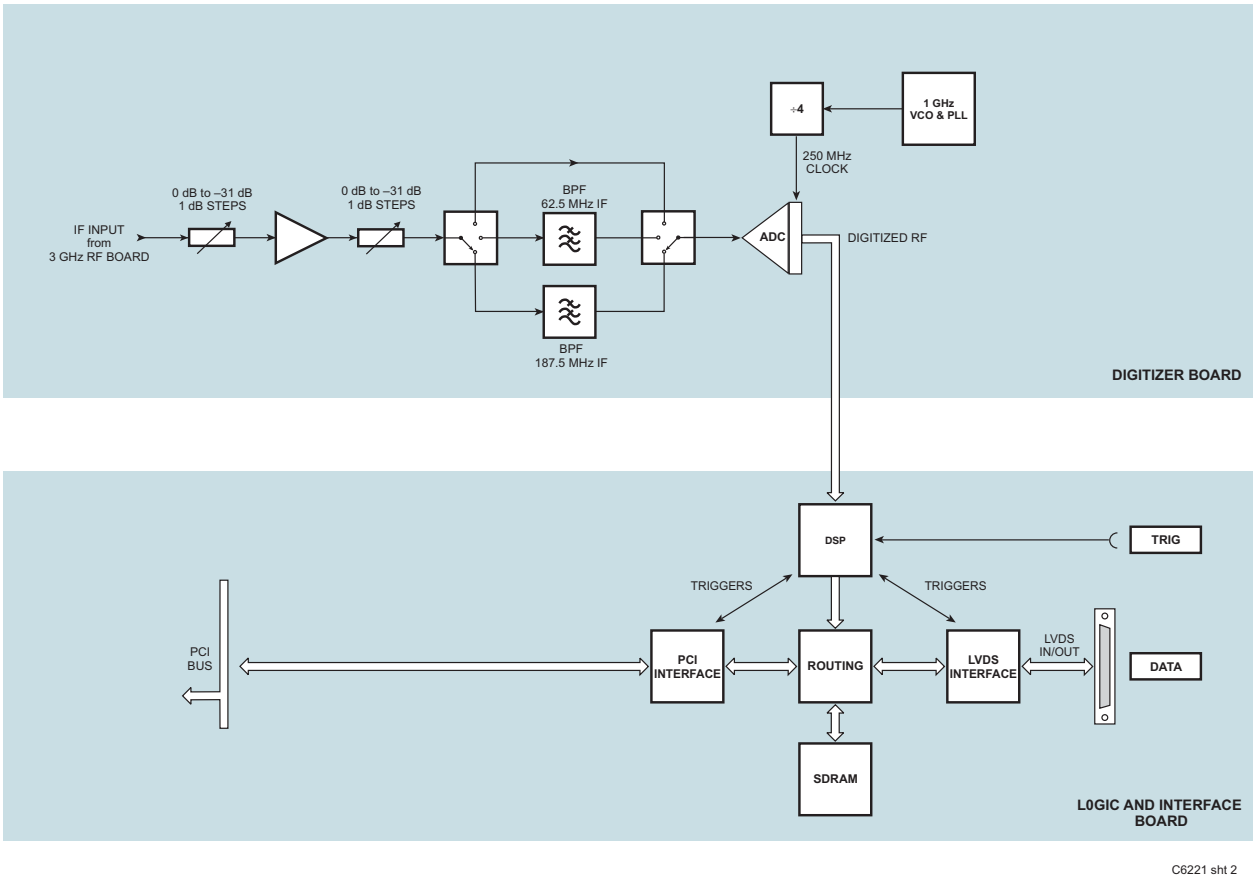
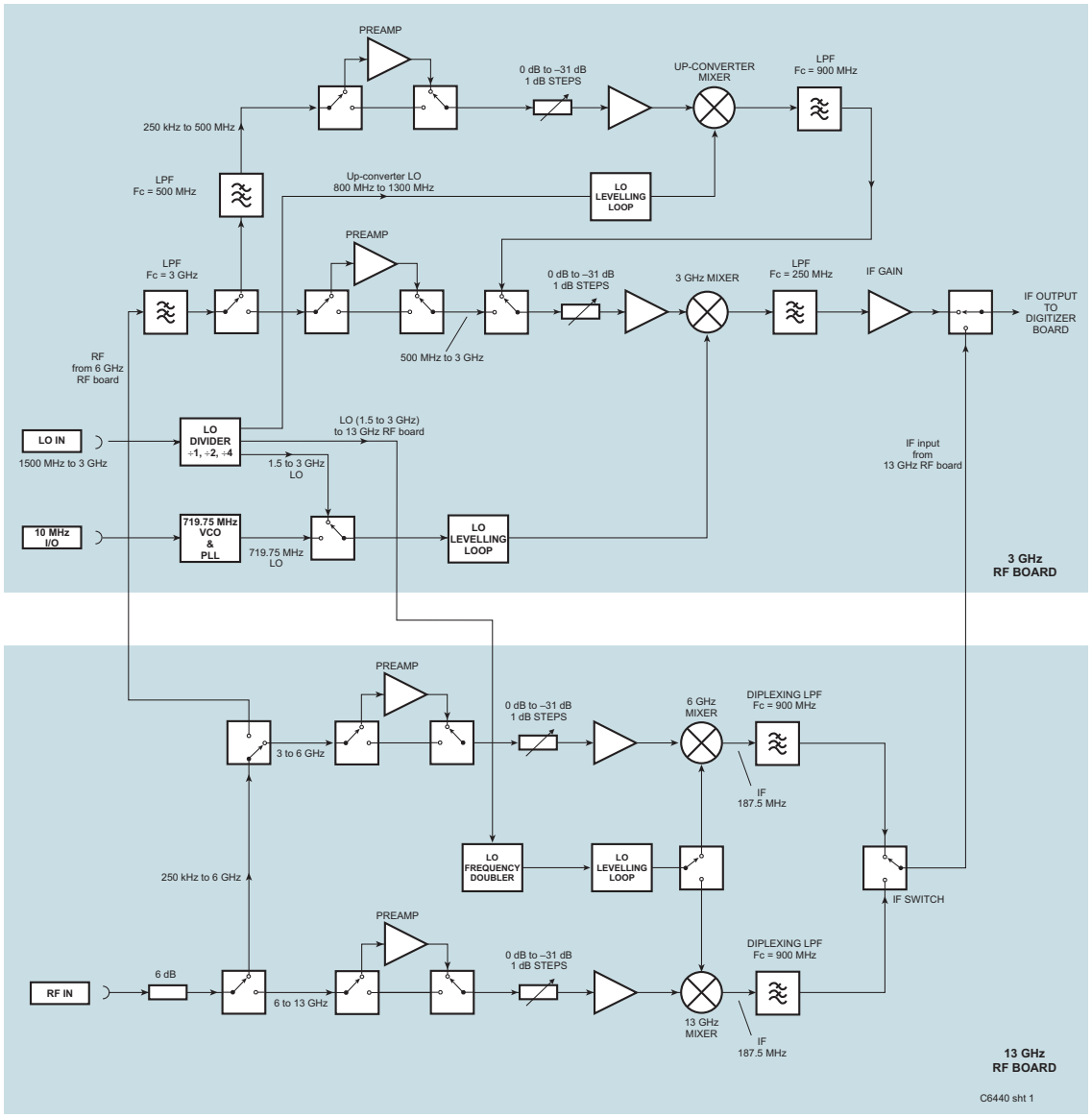


Fig. 35 3035C block schematic diagram


PREAMP
0 dB to –31 dB
1 dB STEPS
UP-CONVERTER
MIXER
LPF
Fc = 900 MHz
250 kHz to 500 MHz
LPF
Fc = 500 MHz
Up-converter LO
800 MHz to 1300 MHz
LO
LEVELLING
LOOP
PREAMP
LPF
Fc = 3 GHz
0 dB to –31 dB
1 dB STEPS
3 GHz MIXER
LPF
Fc = 250 MHz
IF GAIN
IF OUTPUT
TO
DIGITIZER
BOARD
500 MHz to 3 GHz
RF
from 6 GHz
RF board
LO IN
1500 MHz to 3 GHz
LO
DIVIDER
÷1, ÷2, ÷4
LO (1.5 to 3 GHz)
to 13 GHz RF board
1.5 to 3 GHz
LO
IF input
from
13 GHz RF board
10 MHz
I/O
719.75 MHz
VCO
&
PLL
719.75 MHz
LO
LO
LEVELLING
LOOP
3 GHz
RF BOARD
PREAMP
0 dB to –31 dB
1 dB STEPS
6 GHz
MIXER
DIPLEXING LPF
Fc = 900 MHz
3 to 6 GHz
IF
187.5 MHz
LO
FREQUENCY
DOUBLER
LO
LEVELLING
LOOP
IF SWITCH
250 kHz to 6 GHz
PREAMP
6 dB
RF IN
6 to 13 GHz
0 dB to –31 dB
1 dB STEPS
DIPLEXING LPF
Fc = 900 MHz
13 GHz
MIXER
IF
187.5 MHz
13 GHz
RF BOARD
C6440 sht 1

continued…

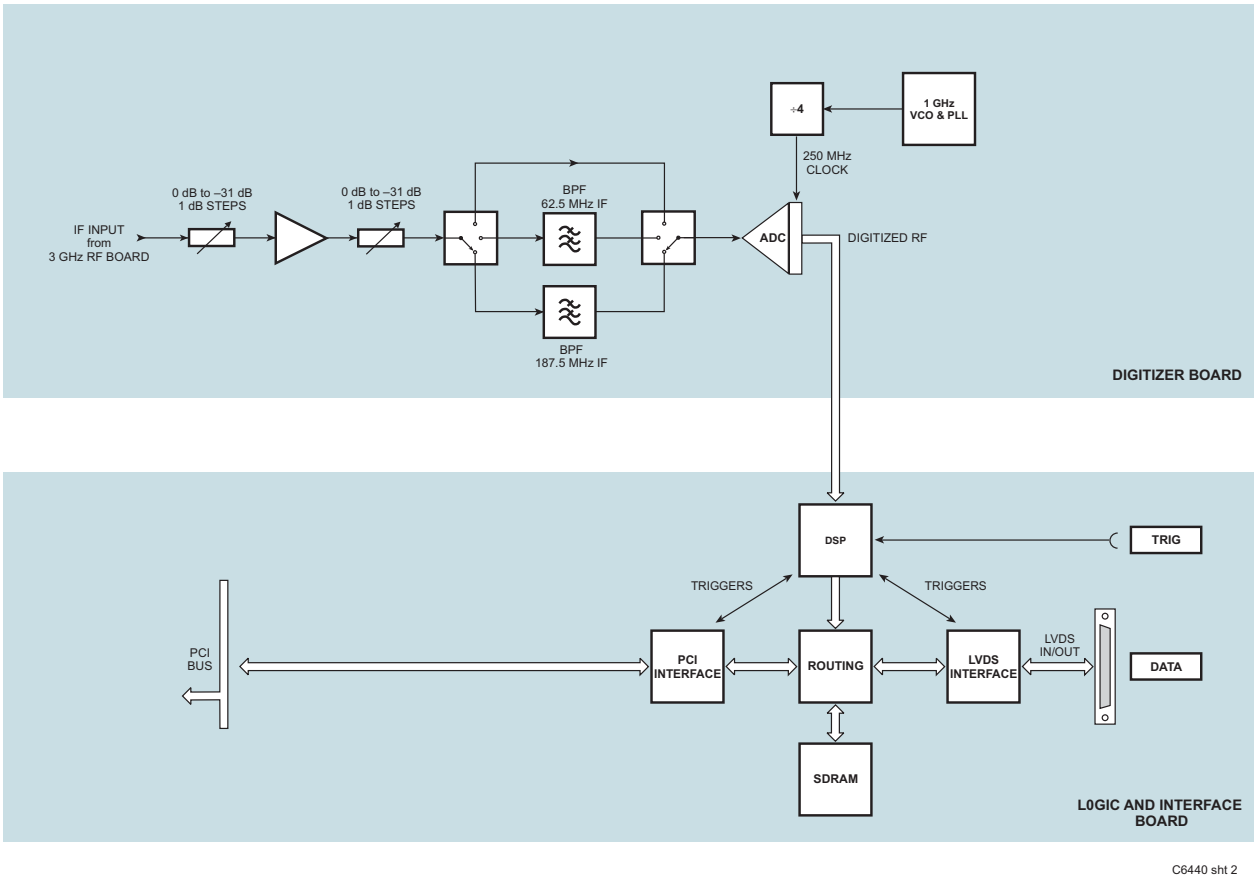


Fig. 36 3036 block schematic diagram

GLOSSARY

ACLR	Adjacent Channel Leakage Ratio: a measurement of transmitter performance for W-CDMA. It is the ratio of transmitted power to the power received (after filtering) in the adjacent RF channel. It describes the amount of distortion generated due to nonlinearities in RF components, and is a critical measurement for CDMA transmitters. Formerly called Adjacent Channel Power Ratio.
ACP(R)	See ACLR.
ADC	An Analog-to-Digital Converter converts a time-varying signal to discrete binary values.
AM	Amplitude Modulation: modulation of the amplitude of a carrier wave.
ARB	Arbitrary Waveform Generator: allows you to edit, generate and play complex recurring waveforms.
ATE	Automatic Test Equipment is program-controlled equipment that tests electronic devices for functionality and performance.
COM	Component Object Model: a way of implementing objects that can be used in environments different from the one they were created in, even across machine boundaries, and independently of language. COM allows the reuse of objects with no knowledge of their internal implementation, as well-defined interfaces are all that is visible to the user.
CW	Continuous Wave: electromagnetic waves, the successive oscillations of which are identical under steady-state conditions, which can be interrupted or modulated to convey information.
DAC	Digital-to-Analog Converter: device that converts a digital code to a time-varying analog signal.
dB	Decibel: a dimensionless logarithmic unit of measurement that expresses the ratio of a power relative to a specified or implied reference level.
dBc	Decibel value specified relative to the carrier level.
dBm	Decibels value specified relative to 1 mW.
DDS	Direct Digital Synthesis: producing an analog waveform — usually a sine wave — by generating a time-varying signal digitally and then performing a digital-to-analog conversion.

dll	dynamic link library: an executable file that allows programs to share code and other resources necessary to perform particular tasks.
EVM	Error Vector Magnitude is used to quantify the performance of a digital radio transmitter or receiver by measuring the deviation of received constellation points from their ideal positions.
FM	Frequency Modulation: modulation of the frequency of a carrier wave.
GND	Ground
GPIB	General Purpose Interface Bus: a parallel interface defined by the IEEE 488 standard, used for attaching sensors and programmable instruments to a computer.
GSM	Global System for Mobile communications: the first all-digital (2G) mobile network.
HF	High Frequency: radio signals in the range 3 MHz to 30 MHz.
IF	Intermediate Frequency: a frequency to which a carrier frequency is shifted as an intermediate step in superheterodyne transmission or reception.
IM(D)	Intermodulation (Distortion): the result of mixing different frequencies together, producing additional signals that are not generally harmonics of the originals.
IQ	In-phase/Quadrature modulation. A modulation scheme where a signal is modulated by two signals 90 degrees out of phase with each other.
LED	Light-Emitting Diode
LO	Local Oscillator**:** an electronic device used to generate a signal normally used to convert a signal of interest to a different frequency using a mixer. See IF.
LVDS	Low-Voltage Differential Signaling: uses a current source to transmit and receive fast signals over simple twisted-pair cable.
MF	Medium Frequency: radio signals in the range 300 kHz to 3 MHz.
PCI	Peripheral Component Interconnect
PM	Phase Modulation: the phase of a carrier is altered by the modulating signal.

PNP	Plug-'N'-Play
PXI	PCI eXtensions for Instrumentation
PXI Express	Backwards compatible with PXI, but providing faster timing and signal lines.
QAM	Quadrature Amplitude Modulation: two amplitude-modulated carriers at the same frequency but at a relative phase angle of 90 degrees are combined in a single channel. This doubles the effective bandwidth of the transmission.
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
RMS	Root Mean Square: the most common mathematical method of defining the effective voltage or current of an AC waveform.
SDRAM	Synchronous Dynamic RAM
SFP	Soft Front Panel: a representation of an instrument's control panel, generated in software, which allows you to control the underlying software and hardware.
SMA	SubMiniature version A (connector)
SMB	SubMiniature version B (connector)
TDMA	Time Division Multiple Access: a digital transmission technology that allows a number of users to access a single RF channel without interference by allocating unique time slots to each user within each channel.
TTL	Transistor-Transistor Logic: switching voltage ranges are V_{OL} = 0.4 V, V_{OH} = 2.4 V, V_{IL} = 0.8 V, V_{IH} = 2.0 V
UHF	Ultra High Frequency: radio signals in the range 300 MHz to 3 GHz.
USB	Universal Serial Bus: a serial bus standard for connecting devices to a host computer, using a standardized interface socket and allowing devices to be connected and disconnected without removing power.

UUT	Unit Under Test
VCO	Voltage-Controlled Oscillator: a frequency generator whose output frequency is a function of an applied voltage. If the applied voltage varies, the output is modulated.
VHDCI	Very High Density Cable Interconnect
VHF	Very High Frequency: radio signals in the range 30 MHz to 300 MHz.
VSWR	Voltage Standing-Wave Ratio: the voltage ratio of the amplitude of a partial standing wave at an antinode (maximum) to the amplitude at an adjacent node (minimum), in a transmission line. A measure of the matching, and efficiency, of transmission devices.
VXI	VMEbus Extension for Instrumentation
WLAN	Wireless Local Area Network: a mobile user can connect to a local area network using a radio signal, over a short distance (usually indoors). Standard IEEE 802.11 defines the technology.
WMAN	Wireless Metropolitan Area Network: a mobile user can connect to a local area network using a radio signal, outdoors. Standard IEEE 802.16 defines the technology.